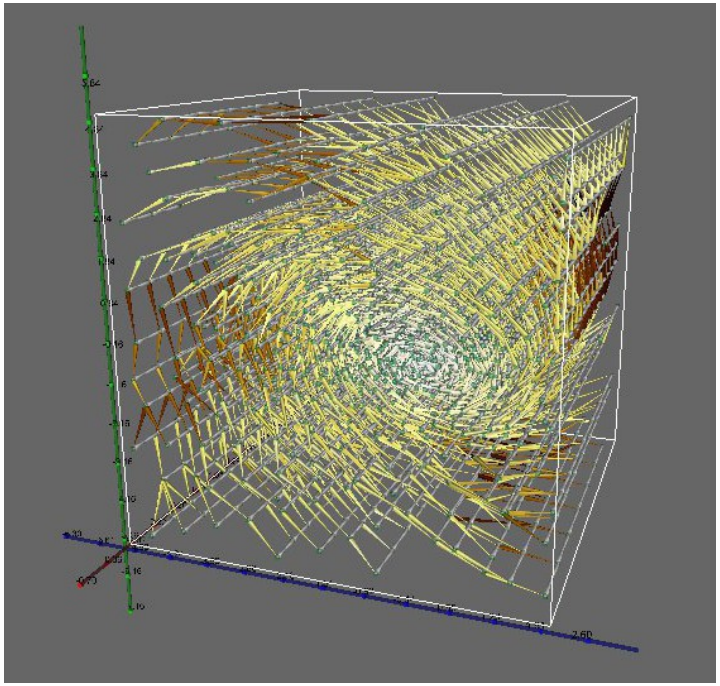
Entwurfsmethodik
Institut für Informatik

FAC '14

A Benchmark Suite for Formal Verification of Analog Circuits



Felix Salfelder, Lars Hedrich

Introduction

MCNC benchmark

- Analog simulation
- Numerical challenges
- Big circuits

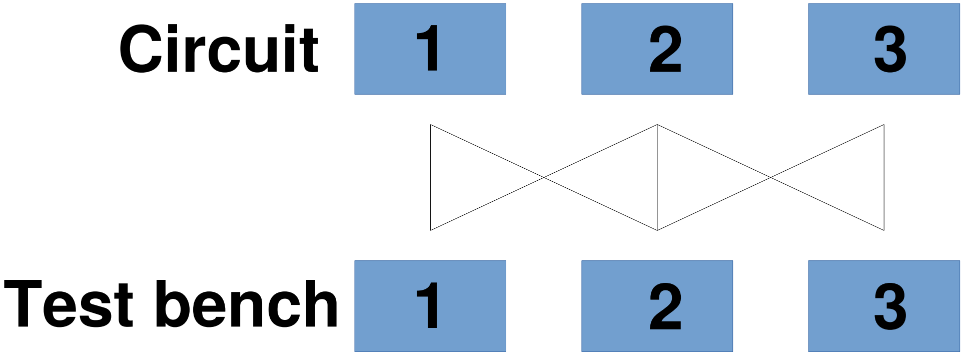
ISCAS'89 benchmark

- Digital circuits
- Simulation, verification

No benchmark available for
cross level behavioural model validation
and model checking

Benchmark Suite for Formal Verification of Analog Circuits

- **Criteria for Selection**
  - Test instances for established methods
  - Challenges for formal methods
  - Proving grounds for new algorithms
  - Portability
  - Pluggability
- **Goals**
  - Share examples
  - Demonstrate results
  - Discussion
    - Terminology
    - Usefulness
    - ...



Supported platforms

Test benches and components are

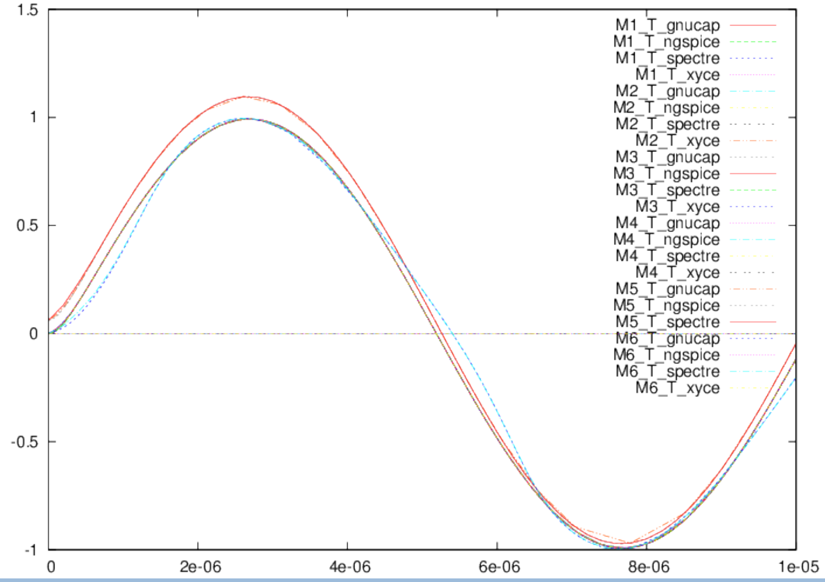
- Spice netlists
- Spice macro models
- Verilog-A modules

PTM parameters for BSIM model

- Parameterset available free of charge
- BSIM supported by most analogue simulators

Verified to work with

- Gnucap
- Spectre (R)
- Ngspice*
- Xyce*

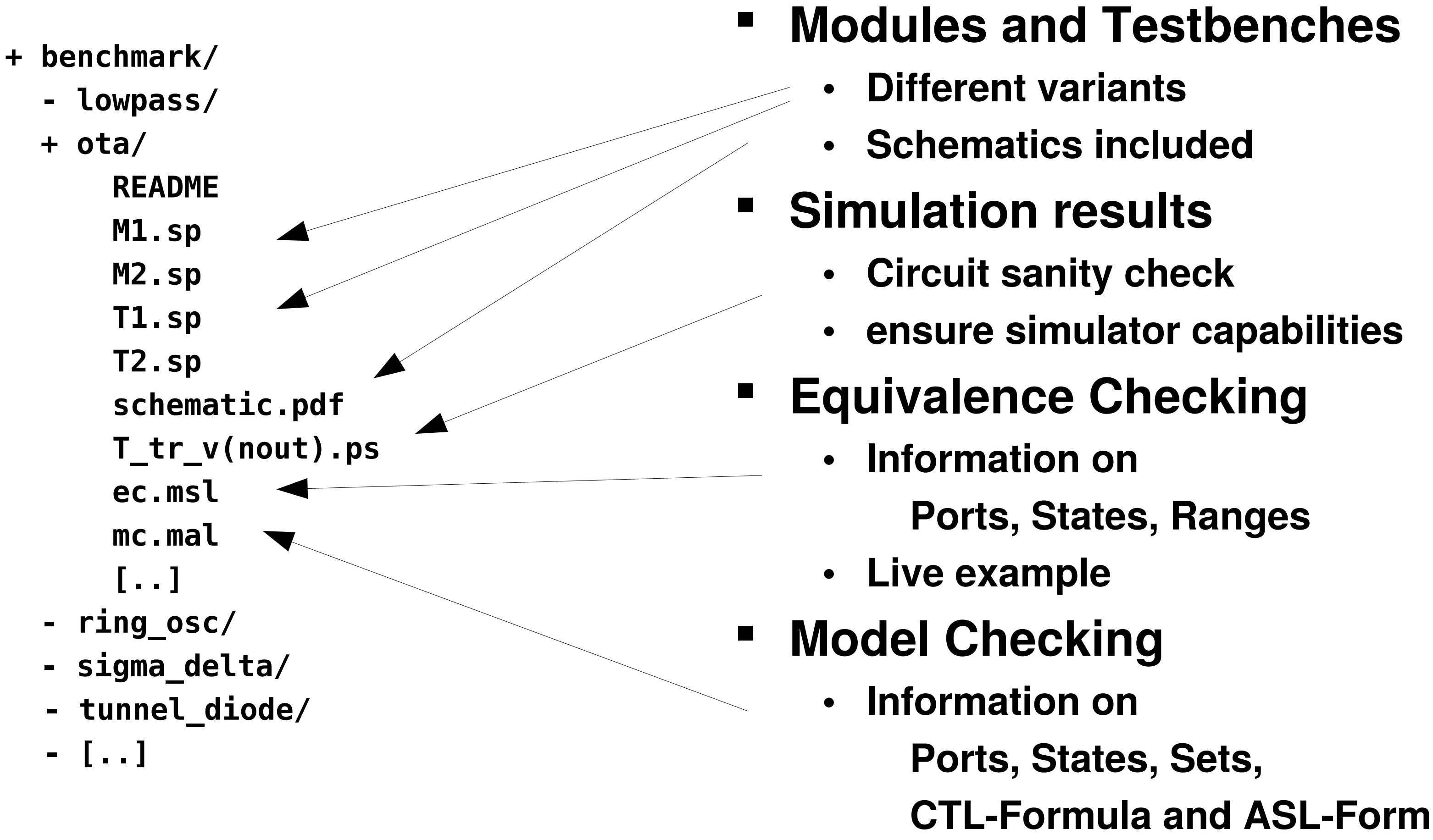


*no Verilog-A

Benchmark Suite: Circuit examples

Class	Architechture	Implementation
4-Pole ring oscillator	CMOS interter cells	BSIM, Spice
Low pass	RC	Spice, Verilog-a
	RL, gyrator+C coil substitute	Spice-macro
	Log domain filter	Spice, BSIM, BJT
	Nonlinear RC	Spice-macro
	OTA, active	Spice
High pass	similar	similar
Band pass	Active (OP)	Spice/BSIM
	Active (OP)	Spice-macro
	Behavioural	Verilog-A
Operational Amplifier	Miller	Spice/BSIM
	Behavioural model	Verilog-A
Operational transconductance amp.	Two stage	Spice/BSIM
	Behavioural model	Verilog-A
Sigma Delta ADC	Second order	Spice-mactro
Inverter, NAND	CMOS	Spice/BSIM
Schmitt trigger	OP/OTA test bench	Spice
Tunnel diode oscillator	TD test bench	Spice-macro

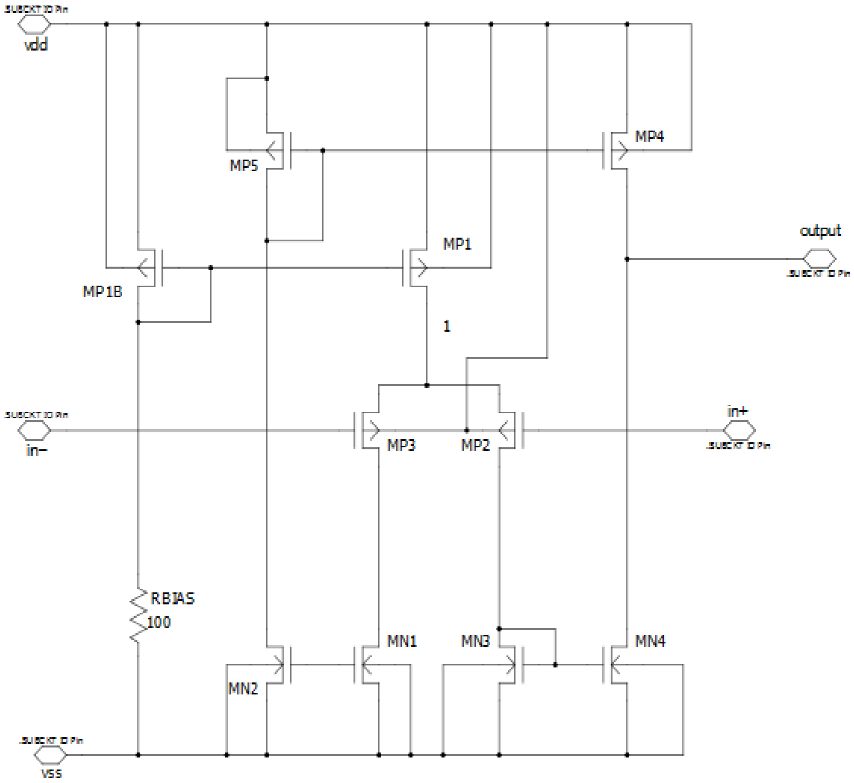
Benchmark Suite: Structure



```
+ benchmark/
  - lowpass/
  + ota/
      README
      M1.sp
      M2.sp
      T1.sp
      T2.sp
      schematic.pdf
      T_tr_v(nout).ps
      ec.msl
      mc.mal
      [..]
  - ring_osc/
  - sigma_delta/
  - tunnel_diode/
  - [..]
```

- **Modules and Testbenches**
  - **Different variants**
  - **Schematics included**
- **Simulation results**
  - **Circuit sanity check**
  - **ensure simulator capabilities**
- **Equivalence Checking**
  - **Information on**
    Ports, States, Ranges
  - **Live example**
- **Model Checking**
  - **Information on**
    Ports, States, Sets,
    CTL-Formula and ASL-Formula

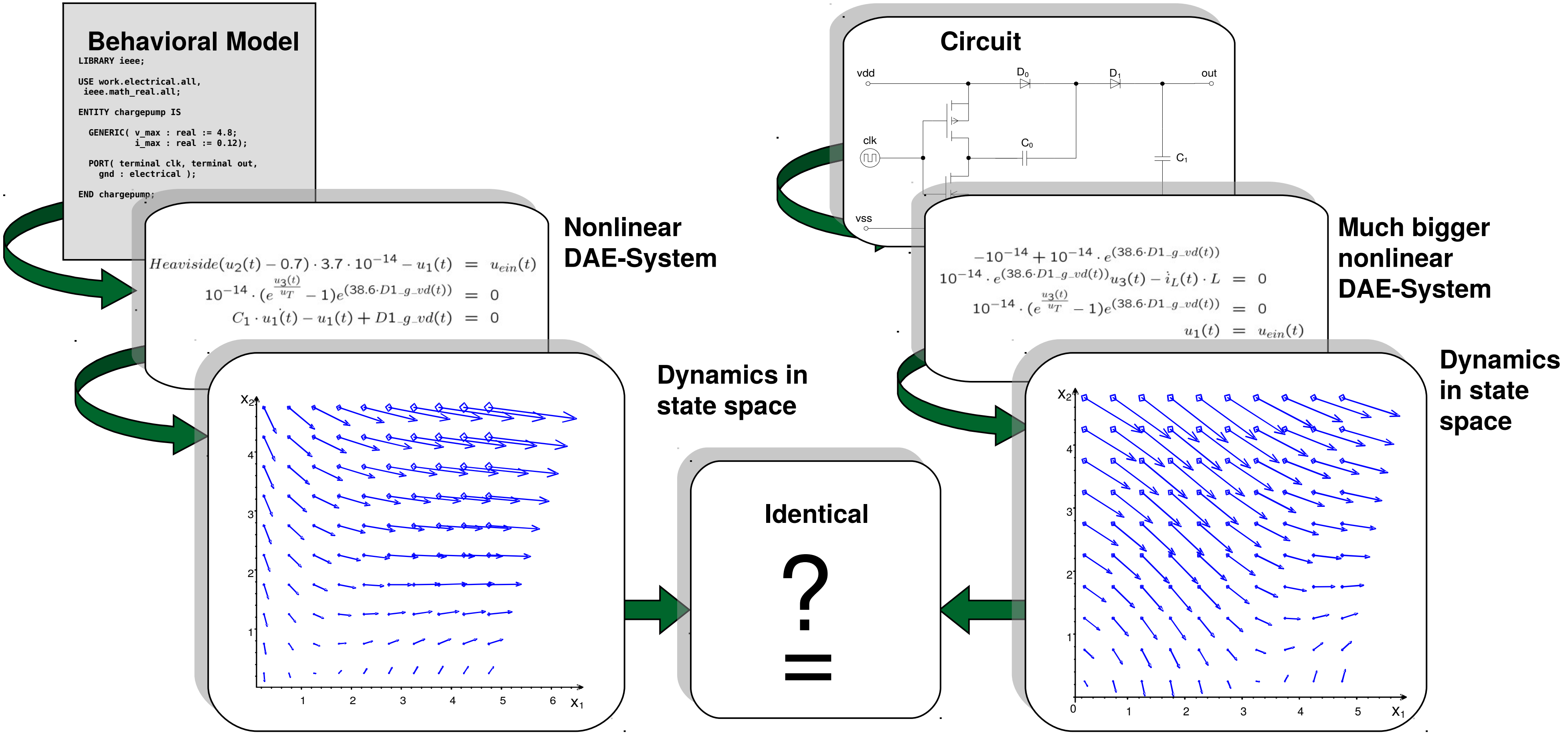
Operational Transconductance Amplifier (OTA)



```
…
analog begin
    I(vddn,out) <+ gm * (V(inp,inn)-voff); // wanted current
    I(vddn,out) <+ cmrr * ((V(inp) +V(inn))/2.0 -
    V(vddp,vddn)/2.0);    // CMRR
    I(out,vddn) <+ V(out,vddn) / rout; // Internal resistor
    I(out,vddp) <+ V(out,vddp) / rout;
    I(out, vddn) <+ C1 *ddt(V(out, vddn) );
    // finite output swing
    if( V(out,vddp) + cloffp  > 0 )
      I(out, vddp) <+ ( V(out,vddp) + cloffp )  / rclamp2;
    if( V(out,vddp) + doff +cloffp > 0  )
      I(out, vddp) <+ (V(out,vddp)+ doff + cloffp) / rclamp;
…
end
```

CMRR (dc)

Equivalence Checking Concept



Behavioral Model

```
LIBRARY ieee;

USE work.electrical.all,
 ieee.math_real.all;

ENTITY chargepump IS

  GENERIC( v_max : real := 4.8;
           i_max : real := 0.12);

  PORT( terminal clk, terminal out,
    gnd : electrical );

END chargepump;
```

$$\begin{aligned} Heaviside(u_2(t) - 0.7) \cdot 3.7 \cdot 10^{-14} - u_1(t) &= u_{ein}(t) \\ 10^{-14} \cdot (e^{\frac{u_3(t)}{u_T}} - 1)e^{(38.6 \cdot D1\_g\_vd(t))} &= 0 \\ C_1 \cdot \dot{u}_1(t) - u_1(t) + D1\_g\_vd(t) &= 0 \end{aligned}$$

Nonlinear DAE-System

Dynamics in state space

Circuit

$$\begin{aligned} -10^{-14} + 10^{-14} \cdot e^{(38.6 \cdot D1\_g\_vd(t))} & \\ 10^{-14} \cdot e^{(38.6 \cdot D1\_g\_vd(t))} u_3(t) - \dot{i}_L(t) \cdot L &= 0 \\ 10^{-14} \cdot (e^{\frac{u_3(t)}{u_T}} - 1)e^{(38.6 \cdot D1\_g\_vd(t))} &= 0 \\ u_1(t) &= u_{ein}(t) \end{aligned}$$

Much bigger nonlinear DAE-System

Dynamics in state space

Identical

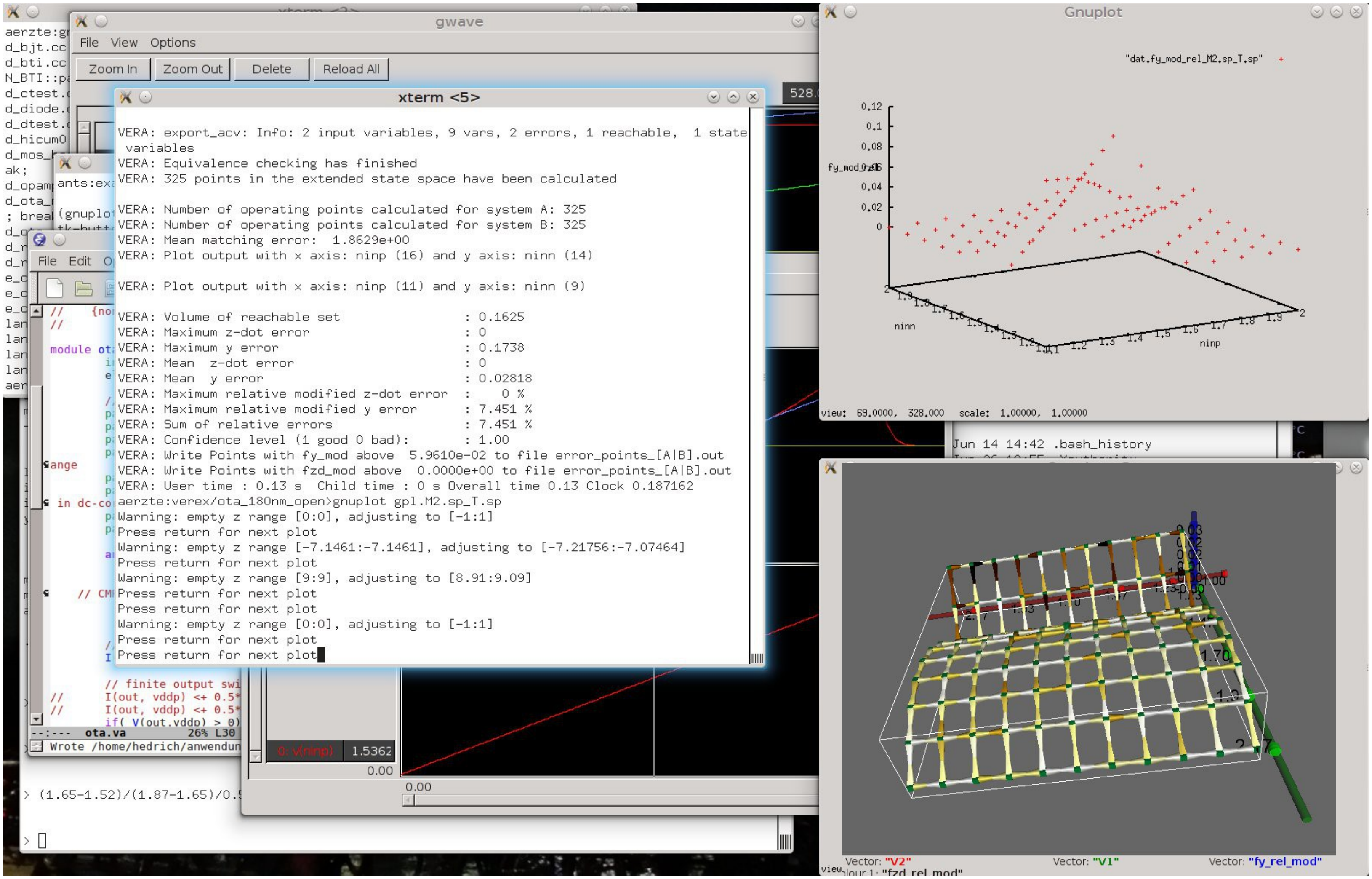
?

=

- Use circuit simulator as beckend.

- 50 equations/transistor
- Implicit, strongly nonlinear equations
- Use of numerical evaluation

Operational Transconductance Amplifier (OTA)



```
VERA: export_acv: Info: 2 input variables, 9 vars, 2 errors, 1 reachable,  1 state
 variables
VERA: Equivalence checking has finished
VERA: 325 points in the extended state space have been calculated

VERA: Number of operating points calculated for system A: 325
VERA: Number of operating points calculated for system B: 325
VERA: Mean matching error:  1.8629e+00
VERA: Plot output with x axis: ninp (16) and y axis: ninn (14)

VERA: Plot output with x axis: ninp (11) and y axis: ninn (9)

VERA: Volume of reachable set                   : 0.1625
VERA: Maximum z-dot error                       : 0
VERA: Maximum y error                           : 0.1738
VERA: Mean  z-dot error                         : 0
VERA: Mean  y error                             : 0.02818
VERA: Maximum relative modified z-dot error     :    0 %
VERA: Maximum relative modified y error         : 7.451 %
VERA: Sum of relative errors                    : 7.451 %
VERA: Confidence level (1 good 0 bad):          : 1.00
VERA: Write Points with fy_mod above  5.9610e-02 to file error_points_[A|B].out
VERA: Write Points with fzd_mod above  0.0000e+00 to file error_points_[A|B].out
VERA: User time : 0.13 s  Child time : 0 s Overall time 0.13 Clock 0.187162
aerzte:verex/ota_180nm_open>gnuplot gpl.M2.sp_T.sp
Warning: empty z range [0:0], adjusting to [-1:1]
Press return for next plot
Warning: empty z range [-7.1461:-7.1461], adjusting to [-7.21756:-7.07464]
Press return for next plot
Warning: empty z range [9:9], adjusting to [8.91:9.09]
Press return for next plot
Press return for next plot
Warning: empty z range [0:0], adjusting to [-1:1]
Press return for next plot
Press return for next plot
```

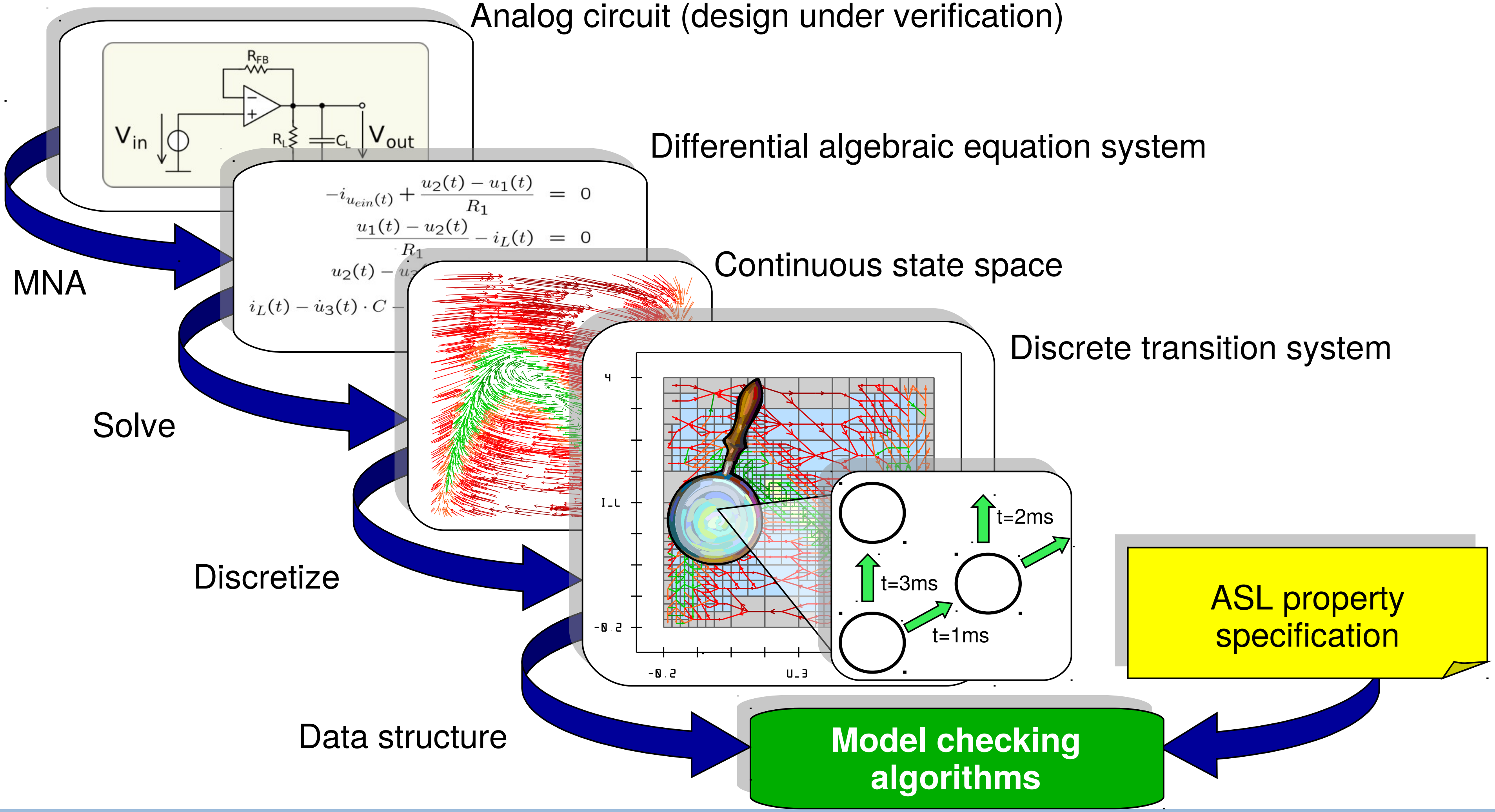
Model checking (low pass filters)

- **MC Properties**
  - Reachable Area
  - Overshoot
  - Gain
  - Slewrate
  - Step response

    … counter examples
- **Variants**
  - RC, LR
  - Nonlinear C RC
  - LR with gyrator and Cap
  - Logdomain
  - OTA (active)

```
# Reachable states
fix = steadystates;
reachable = EF^-1 fix;

# Reachable states from  -0.1 < Uin < 0.1
uslice = nin[<0.11] and nin[>-0.11];

ulow = nin[<-0.09] and nin[>-0.11];
uhigh = nin[<0.11] and nin[>0.09];

reachin = on uslice reach from fix;

# overshoot
overshoot = reachin and nout[> 0.12];
undershoot = reachin and nout[< -0.12];

# dc-gain of odB:
calculation gain_calc("(calc_par3 – calc_par4)/  \
                       (calc_par1 - calc_par2)");

numvar %gainmin,%gainmax;
on fix assign(%gainmin,min)
    gain_calc(nin,0,nout,0)[-inf,inf];
on fix assign(%gainmax,max)
    gain_calc(nin,0,nout,0)[-inf,inf];

for %gainmin assert [ 0.8, 1.2 ];
for %gainmax assert [ 0.8, 1.2 ];

[..]
```

Model Checking Flow



Analog circuit (design under verification)

Differential algebraic equation system

Continuous state space

Discrete transition system

MNA

Solve

Discretize

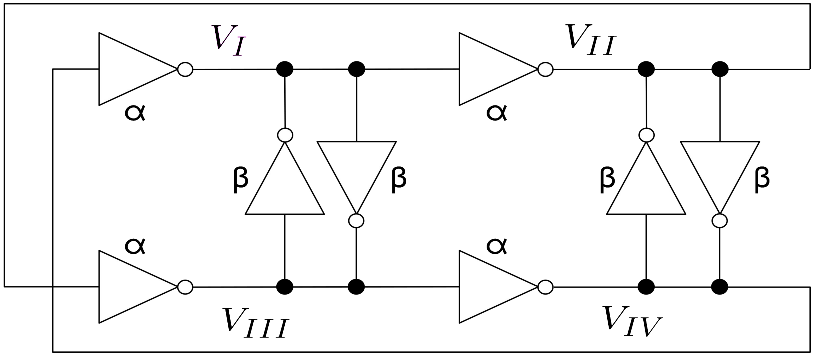
Data structure

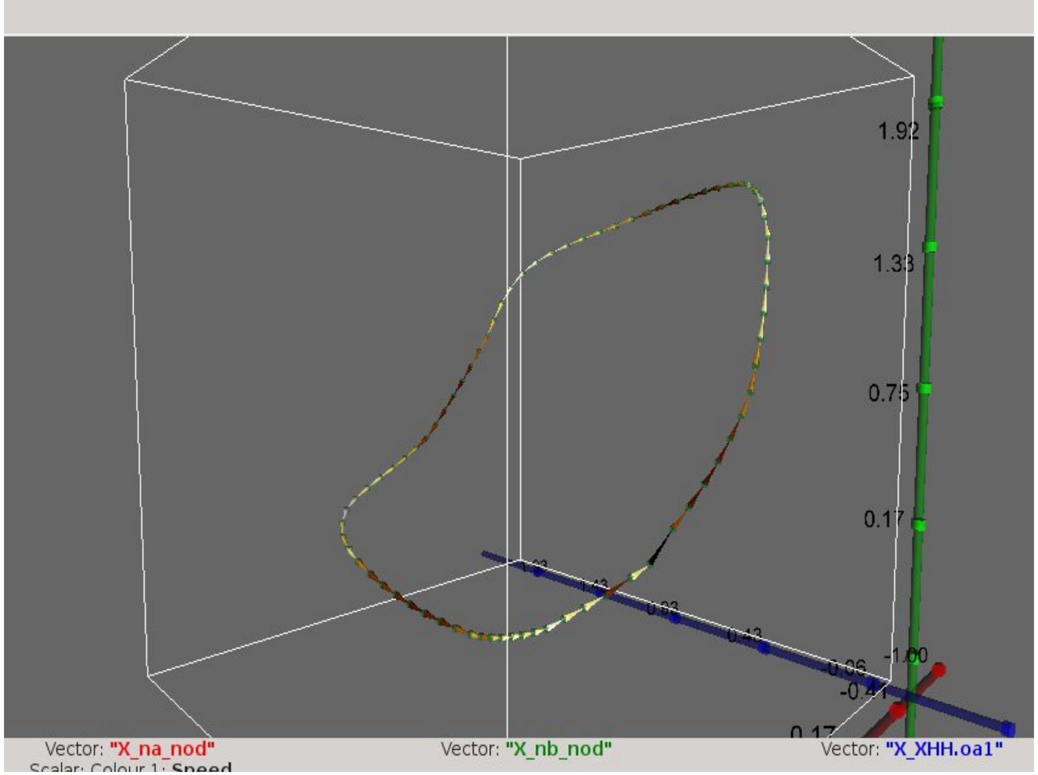
ASL property specification

Model checking algorithms

R_{FB}
V_{in}
R_L
C_L
V_{out}
$-i_{u_{ein}}(t) + \frac{u_2(t) - u_1(t)}{R_1} = 0$
$\frac{u_1(t) - u_2(t)}{R_1} - i_L(t) = 0$
$u_2(t) - u$
$i_L(t) - \dot{u}_3(t) \cdot C -$
4
I_L
-0.2
-0.2
U_3
t=2ms
t=3ms
t=1ms

4-Pole Oscillator at α/β = 2.4

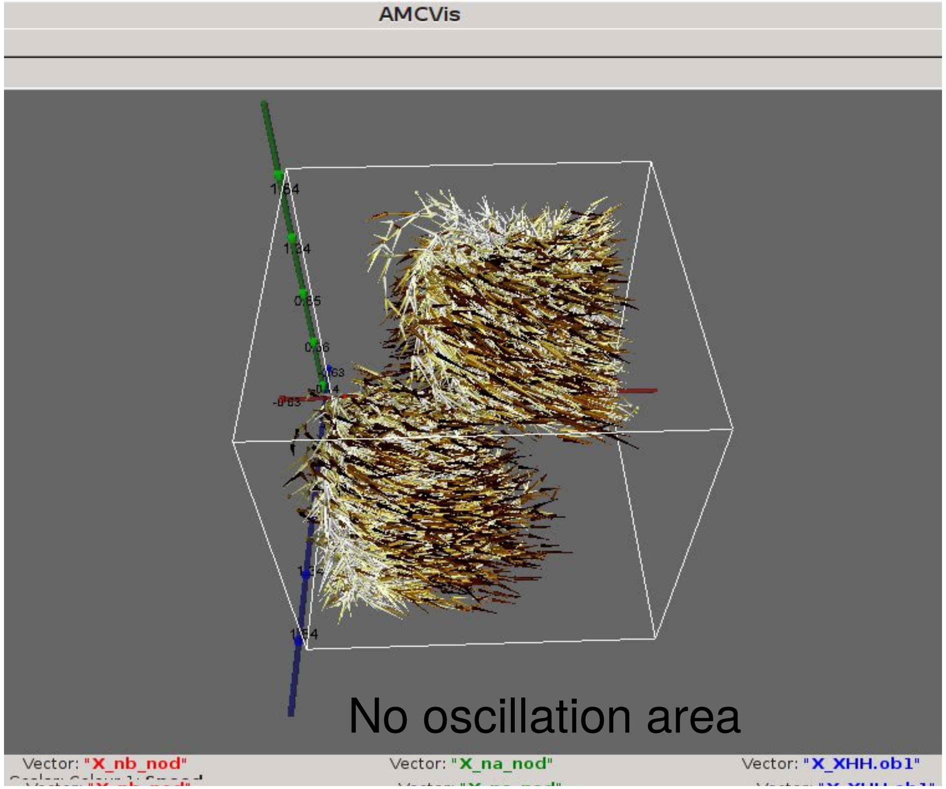




Vector: "X_na_nod" Vector: "X_nb_nod" Vector: "X_XHH.oa1"

Scalar: Colour 1: Speed

Oscillation trajectory



AMCVis

No oscillation area

Vector: "X_nb_nod" Vector: "X_na_nod" Vector: "X_XHH.ob1"

Conclusion

- Benchmark suite available*
- Key issues addressed
  - Model checking
  - Equivalence Checking
  - Transistor and behavioural level
- Unaddressed Problems
  - Process Variablility
  - Mixed Signal
  - System Level

*http://www.em.cs.uni-frankfurt.de/FAC14/benchmark

Thank You