Model-Based Synthesis of High-Speed Serial-Link Transmitter Designs

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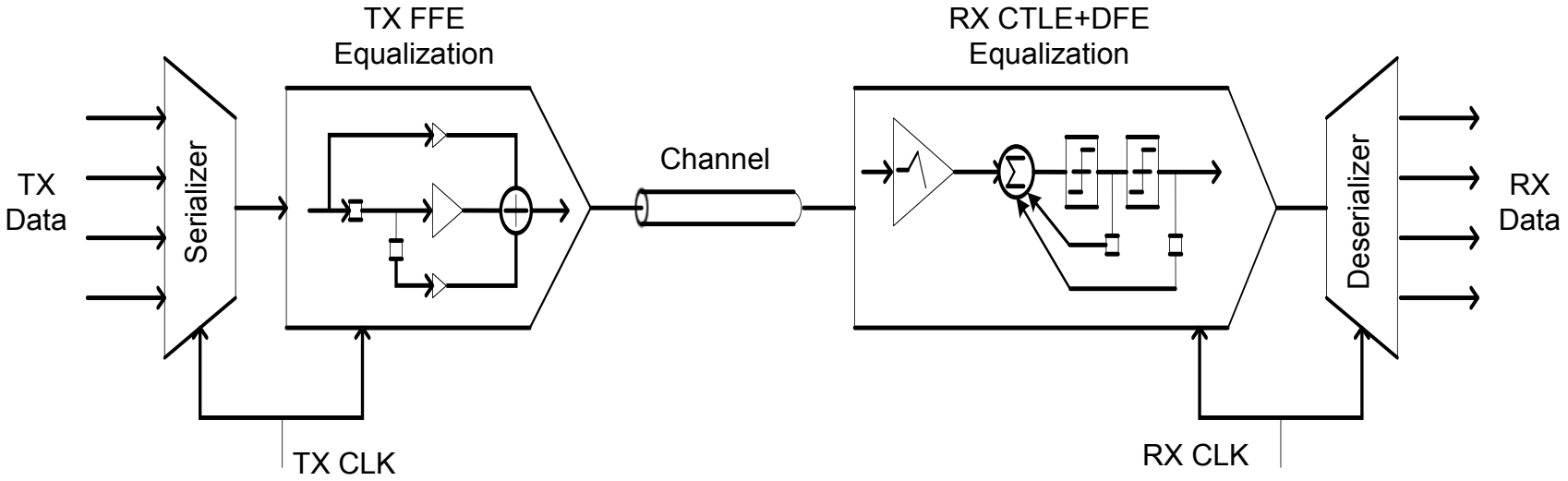
Outline

- Introduction
  - High-Speed Serial-link transmitter
  - Geometric Programming (GP)
- Model-based Design Framework(CML)
  - Transistor Level Modeling
  - Circuit Level Modeling
  - Numerical Experiments for Model Validation
  - Hierarchical Modeling
- System Level Optimization
- Conclusion

Introduction



- High-speed links are common building blocks in consumer electronics.
- Many link systems are designed using current-mode logic(CML) circuits.
  - CML Buffer, Latch, Multiplexer…
- Lack of automated design flow prohibits efficient design reuse of links

➢ Our goal: To provide an design synthesis flow for CML-style circuits

Introduction

- **Geometric programming (GP)**

$$\begin{aligned} &\text{minimize } f_o(x) \\ &\text{subject to} \quad f_i(x) \le 1, \quad i = 1, \dots, m \\ &\qquad\qquad\ \ g_i(x) = 1, \quad i = 1, \dots, p \end{aligned}$$

where f_i are posynomials, g_i are monomials

monomial : $g(x) = c{x_1}^{\alpha_1}{x_2}^{\alpha_2}\cdots{x_n}^{\alpha_n}$ with $c > 0, \alpha_i \in \mathbb{R}$

posynomial : $f(x) = \sum_{k=1}^{N} c_k {x_1}^{\alpha_{1k}}{x_2}^{\alpha_{2k}}\cdots{x_n}^{\alpha_{nk}}$ with $c_k > 0, \alpha_{ik} \in \mathbb{R}$

- **Model-based synthesis via geometric programming[1][2]**
  - Computationally efficient
  - Scalable to a hierarchical design with inter-block dependency
  - Seamless design porting over process and technology
  - Challenge: accurate circuit-level model compatible with GP

[1] M. Hershenson, et al, “Optimal design of a CMOS opamp via geometric programming,” IEEE TCAD. 2001
[2] D. M. Colleran, et al, “Optimization of phase-locked loop circuits via geometric programming,” CICC2003.

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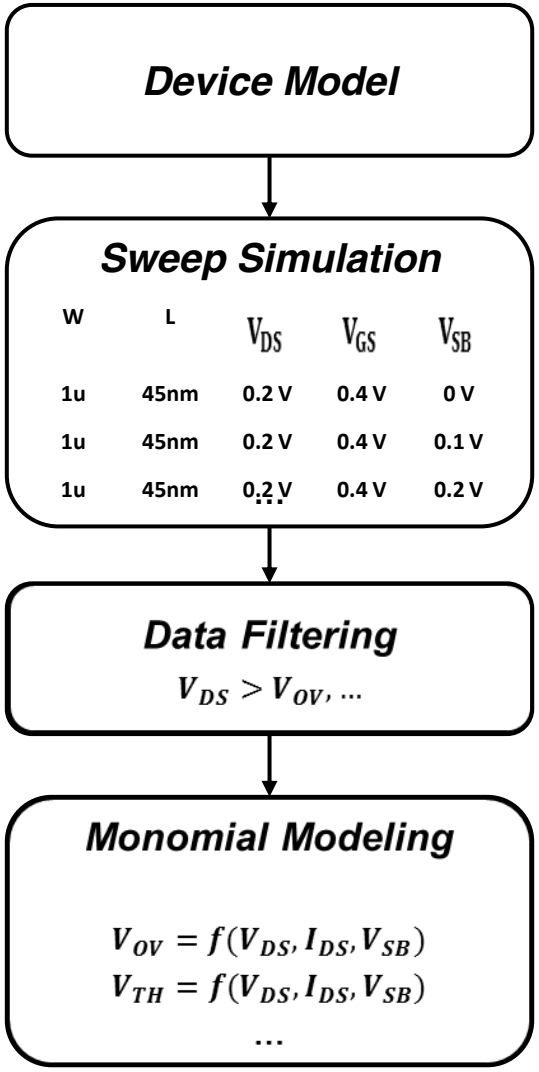
Transistor Level Modeling



Process Design Kit (PDK)
or
Predictive Technology Models (PTM)

Run SPICE simulation by sweeping node voltage of transistor

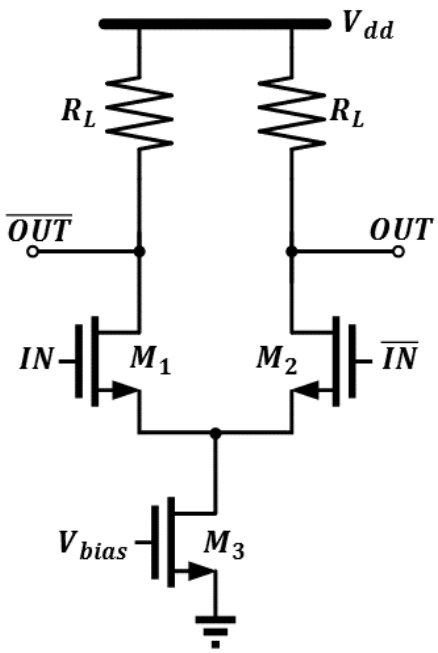
Screen the simulation data for valid transistor operation region (saturation …)

Monomial formula for transistor models

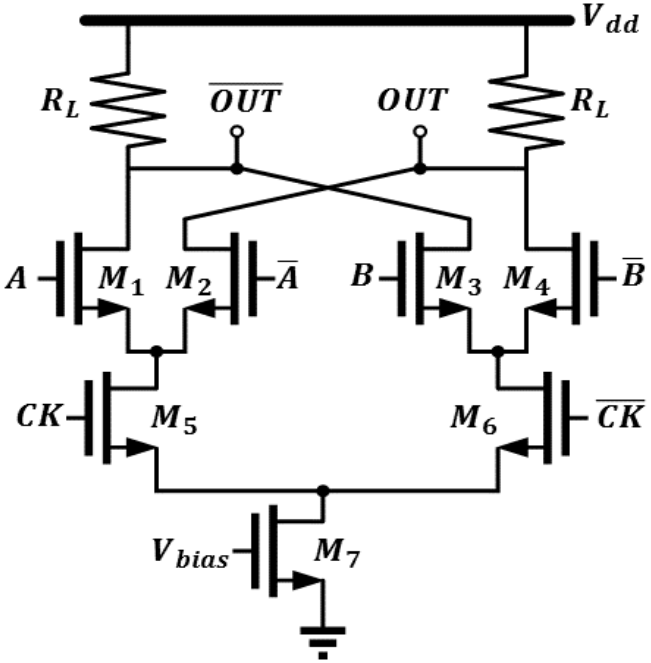
$$V_{OV}, V_{TH} = a_1 {V_{DS}}^{a_2} {I_{DS}}^{a_3} {V_{SB}}^{a_4}$$
$$C_{gg}, C_{ss}, C_{dd} = m \cdot b_1 {V_{DS}}^{b_2} {I_{DS}}^{b_3} {V_{SB}}^{b_4}$$
$$g_m, g_{ds} = m \cdot c_1 {V_{DS}}^{c_2} {I_{DS}}^{c_3} {V_{SB}}^{c_4}$$

[3] J. Kim, et al, “Convex piecewise-linear modeling method for circuit optimization via geometric programming,” IEEE TCAD. 2010

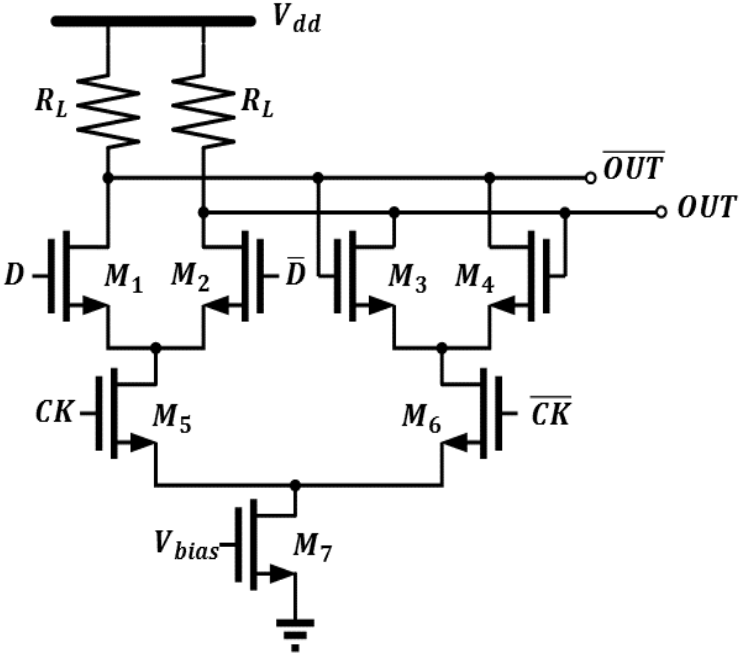
Circuit Level Modeling



Buffer



MUX



Latch

- CML-circuit models should include
  - Bias constraints: to ensure full-steering of bias current
  - Delay models: to estimate propagation delay

Bias constraints

Dimension constraints

$$W_1 = W_2, L_1 = L_2 = L_{min}$$
$$\dots$$

Bias modeling

$$I_1 = I_2 = 0.5I_3$$
$$V_{OV3} + V_{TH3} \le V_{bias}$$
$$V_{DS3} + V_{OV1} + V_{TH1} \le V_{icm}$$
$$V_{DS3} + V_{DS1} + 0.5I_3R_L \le V_{dd}$$
$$\dots$$

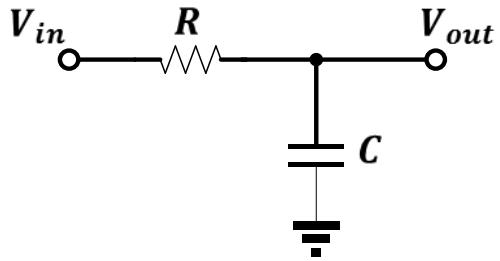
Performance parameters

$$A_v = g_{m1}R_L$$
$$Power = V_{dd} \times I_3$$
$$Area = 2\alpha_0 R_L + \alpha_1 \sum_{i=1}^{N} W_i L_i$$
$$\tau = R_L(C_L + C_{dd1}) + (C_{ss1} + C_{dd3})/g_{m3}$$
$$\dots$$

Operating conditions

$$V_{OV1} \le V_{DS1}, V_{OV3} \le V_{DS3}$$
$$\sqrt{2}V_{OV1} \le V_{id}$$
$$\dots$$

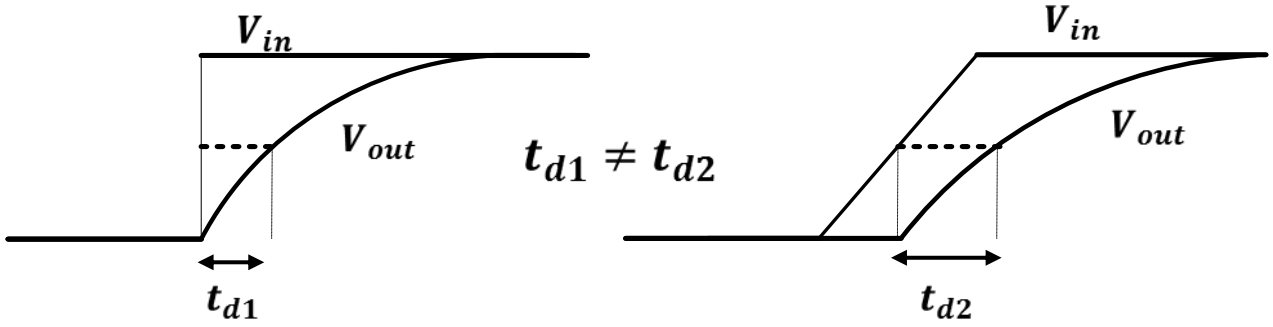
CML Gate Delay Model



$$t_d = ln(2) \cdot \tau \approx 0.6933\tau = 0.6933RC$$

- Simple RC delay model cannot reflect practical signal transition in high-speed serial-link systems[4].

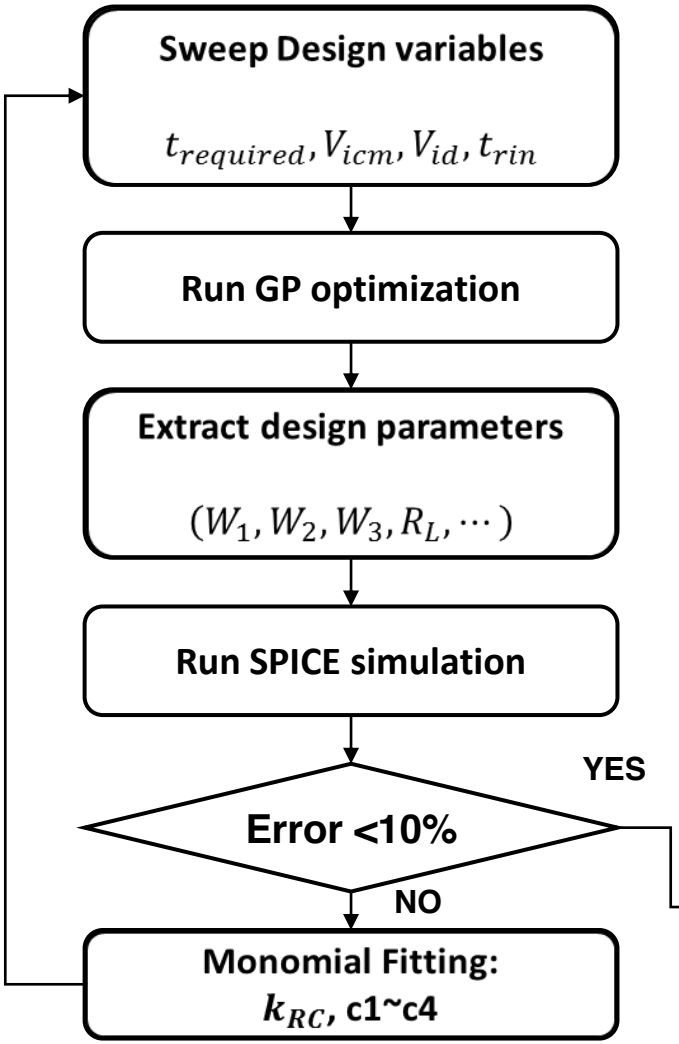
- Finite input slope effects should be included in delay models.



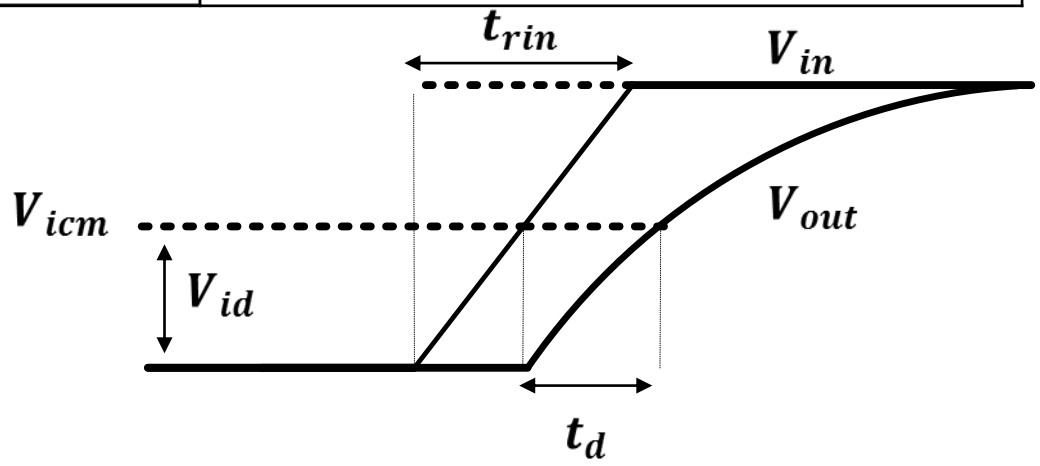
- Earlier CML gate delay models[5] do not have GP compatible forms.

[4] H. Hassan, et al, "MOS current mode circuits: Analysis, Design and Variability," IEEE TVLSI 2005
[5] U. Seckin, et al, " A Comprehensive Delay Model for CMOS CML Circuits," IEEE TCAS. I . 2008

CML Gate Delay Model



Variables	Description
$t_{required}$	Timing margin
V_{icm}	Input CM voltage
V_{id}	Input differential voltage
t_{rin}	Input rise time



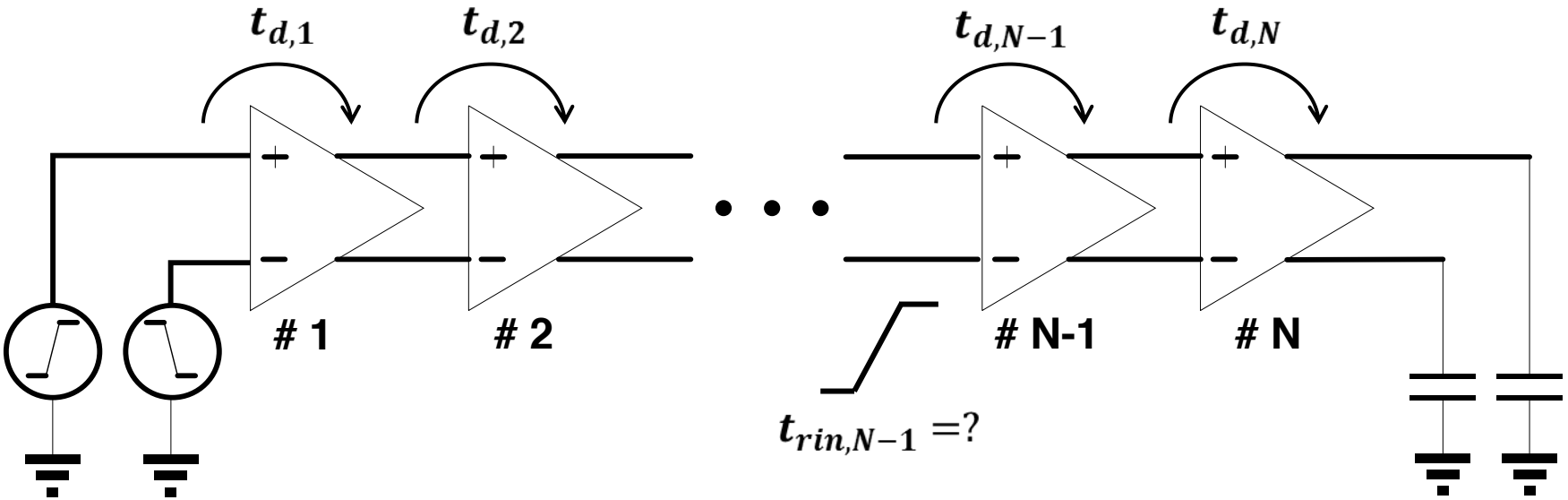
$$t_d = k_{RC}\tau = c_1 {V_{id}}^{c_2} {t_{required}}^{c_3} {t_{rin}}^{c_4} \tau$$

($c_1 \sim c_4$: fitting parameters of delay model)

[6] S. Y. Kim, et al, "Closed-form RC and RLC delay models considering input rise time," IEEE TCAS. Ⅰ. 2007
[7] R. Mita, et al, "Propagation delay of a RC chain with a ramp input," IEEE TCAS. Ⅱ. 2007

CML Gate Delay Model

- **Output rise time models**

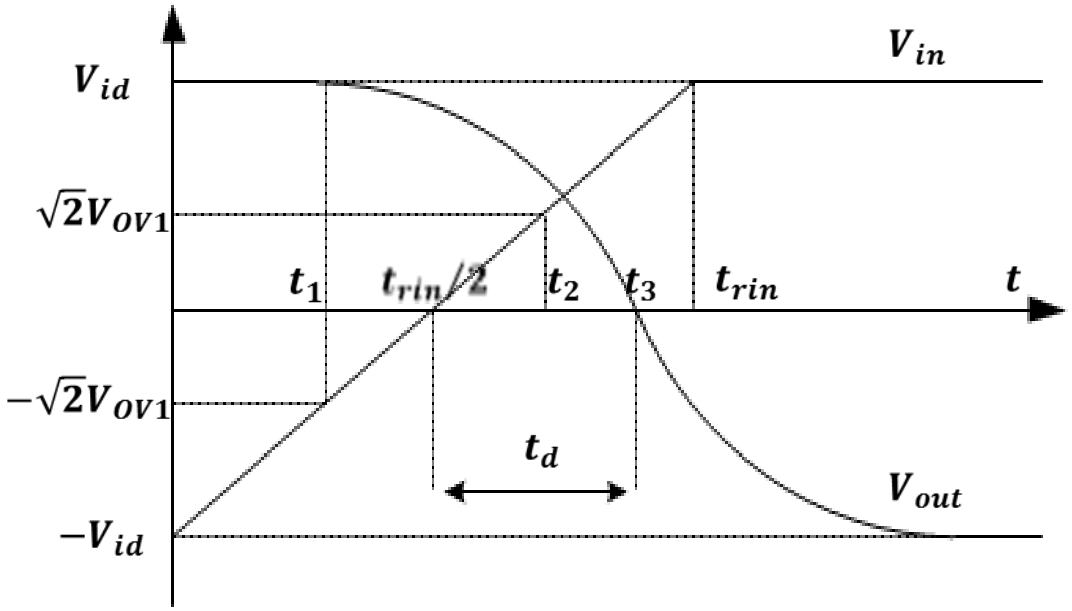


Newly proposed delay model need exact input rise time

- For design synthesis of cascaded CML-based circuits, output rise time should be estimated.

CML Gate Delay Model

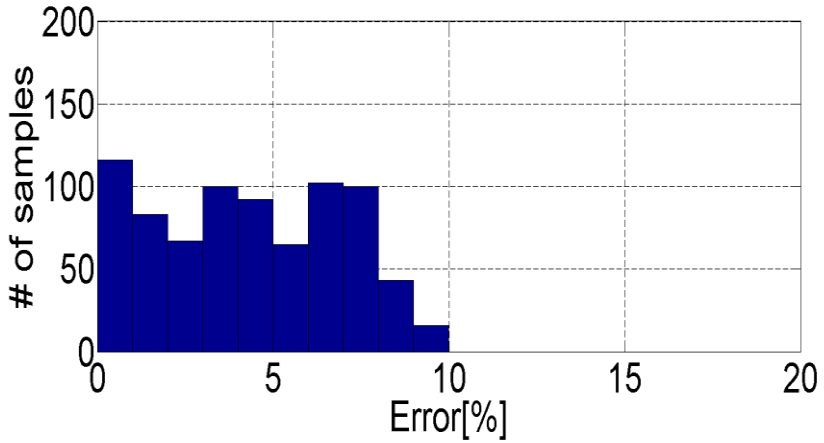
- **Output rise time models**



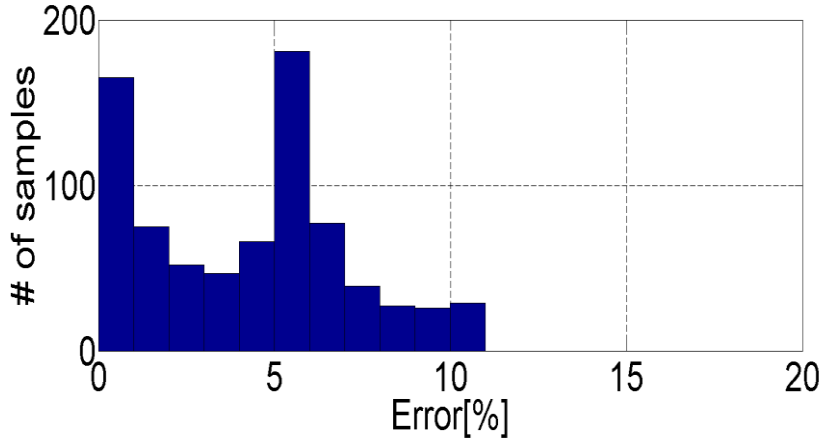
$$t_{rout} = 2(t_3 - t_1) = 2\left(t_3 - \frac{1}{2}t_{rin} + \frac{1}{2}t_{rin} - t_1\right)$$

$$= 2\left(t_d + \frac{\sqrt{2}V_{OV1}}{2V_{id}}t_{rin}\right) \approx a_1\left(\frac{\sqrt{2}V_{OV1}}{2V_{id}}t_{rin}\right)^{a_2} {t_d}^{a_3}$$

Numerical Simulation for Model Validation



(a)



(b)

Modeling error statistics of CML buffer
(a) t_d (b) t_{rout}

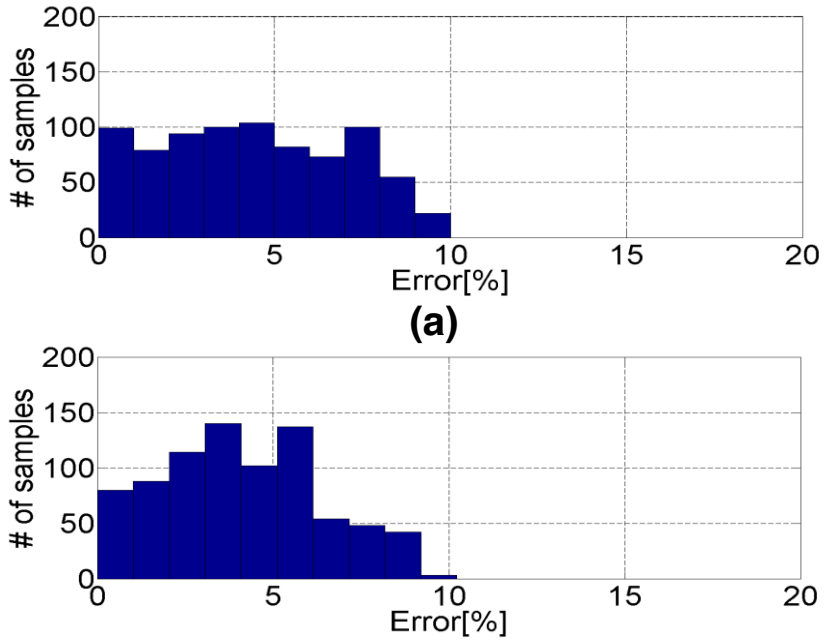
Process Design Kit(PDK)

– Predictive Technology Model 45nm

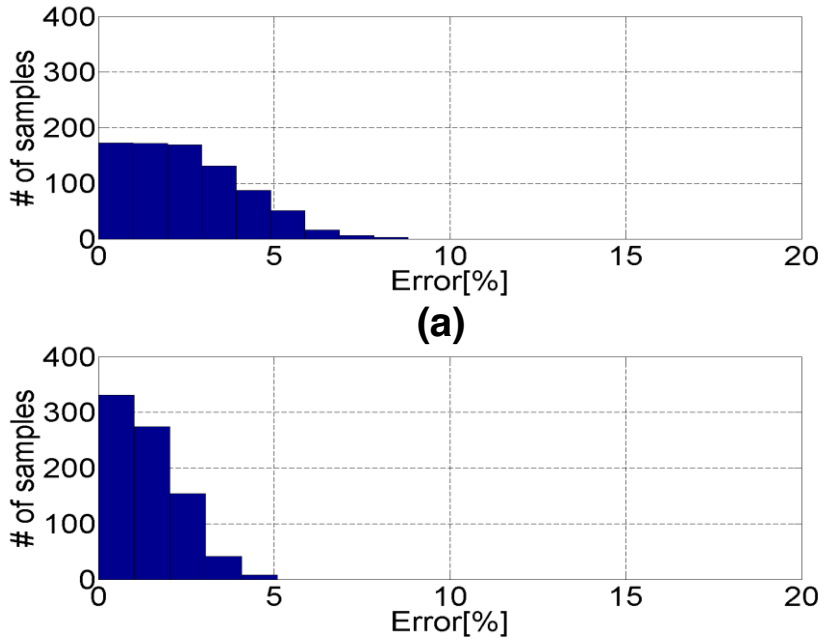
Mean/Max modeling error of CML buffer

Variable /Sweep Range	$V_{icm} = [0.8, 0.95]$, $V_{id} = [0.3, 0.15]$ $t_{required} = [10\ \text{ps}, 100\ \text{ps}]$ $t_{rin} = [10\ \text{ps}, 300\ \text{ps}]$
Property	Mean/Max modeling error[%]
t_d	4.34/10.00
t_{rout}	4.23/11.00

Numerical Simulation for Model Validation



Modeling error statistics of CML multiplexer (a) t_d (b) t_{rout}

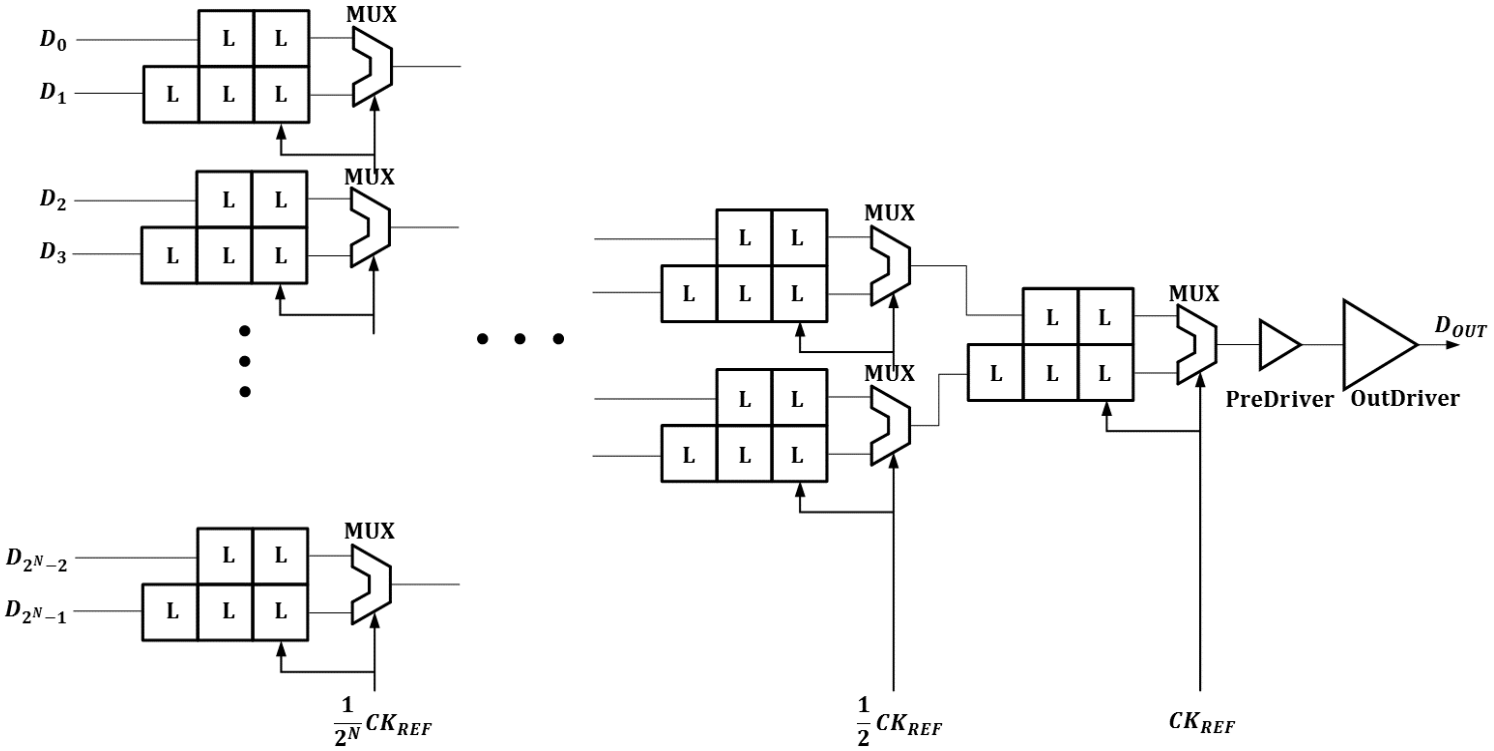


Modeling error statistics of CML latch (a) $t_{rout,c2q}$ (b) $t_{rout,d2q}$

Property	Mean/Max modeling error[%]
t_d	4.45/10.00
t_{rout}	4.11/10.22

Property	Mean/Max modeling error[%]
$t_{rout,c2q}$	2.48/8.82
$t_{rout,d2q}$	1.40/5.09

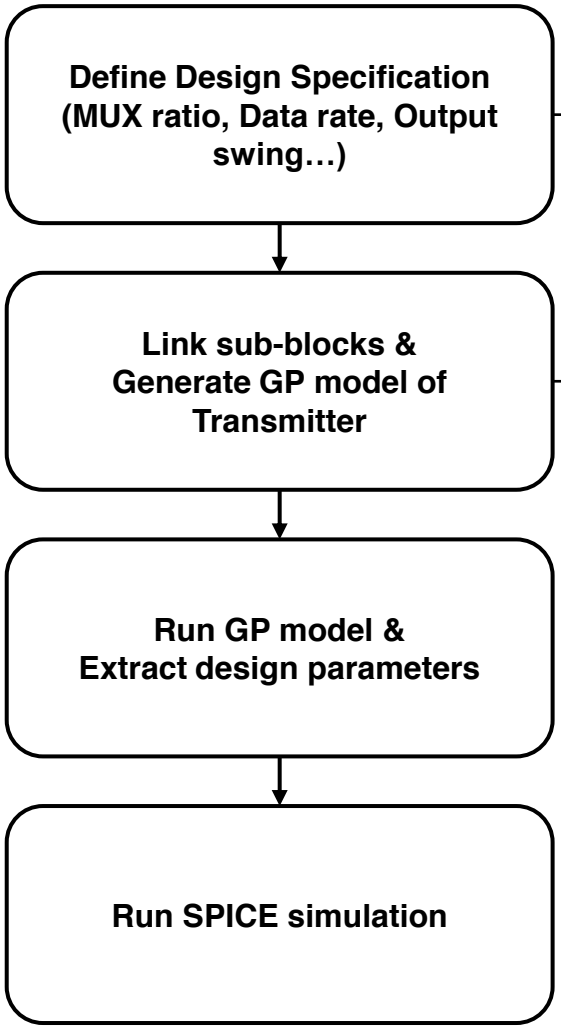
Hierarchical Modeling



Architecture of transmitter with 2^N:1 serializer

- To use unit CML gates as standard cell, dependency of all adjacent inter-nodes should be considered: capacitance loading, voltage swing

Hierarchical Modeling



Variables	Description
N	Number of stage
DR	Data rate
$V_{out,min}$	Minimum single-ended output voltage swing
Area_{max}	Maximum area allowed for design
C_{out}	Final output load capacitance

```
for k=1:N do
  Cload.latch(k)==Cin.mux(k)
  Vin_swing.mux(k)==Vout_swing.latch(k)
  if n≠N then
    Cload.mux(k)==Cin.latch(k+1)
    Vin_swing.latch(k+1)==Vout_swing.mux(k)
  end if
end for
Cload.mux(N)==Cin.predriver
Cload.predriver=Cin.outdriver
Cload.outdriver=Cout
Vin_swing.predriver==Vout_swing.mux(N)
Vin_swing.outdriver==Vout_swing.predriver
tin_rise.predriver==tout_rise.mux(N)
tin_rise.outdriver==tout_rise.predriver
```

⇒**Modeling code for inter-node dependency**

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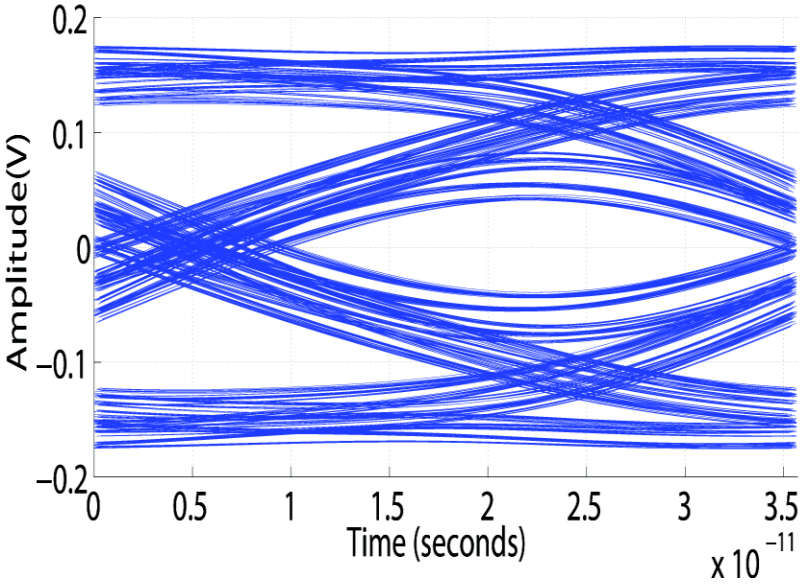
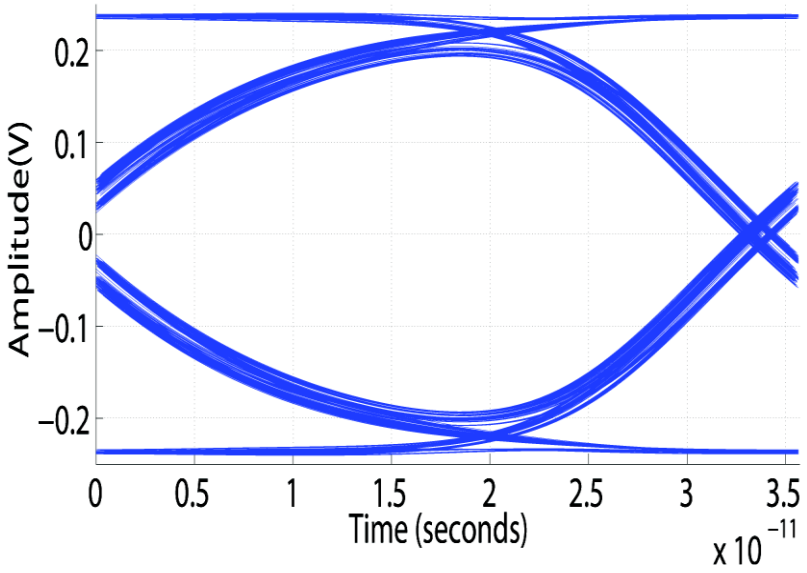
Comparison with simple RC Model

	Design specifications
MUX ratio	8:1
Data rate	28 Gb/s
V_{ppd}	≥ 400 mV
$t_{rin,ck}/T$	0.4

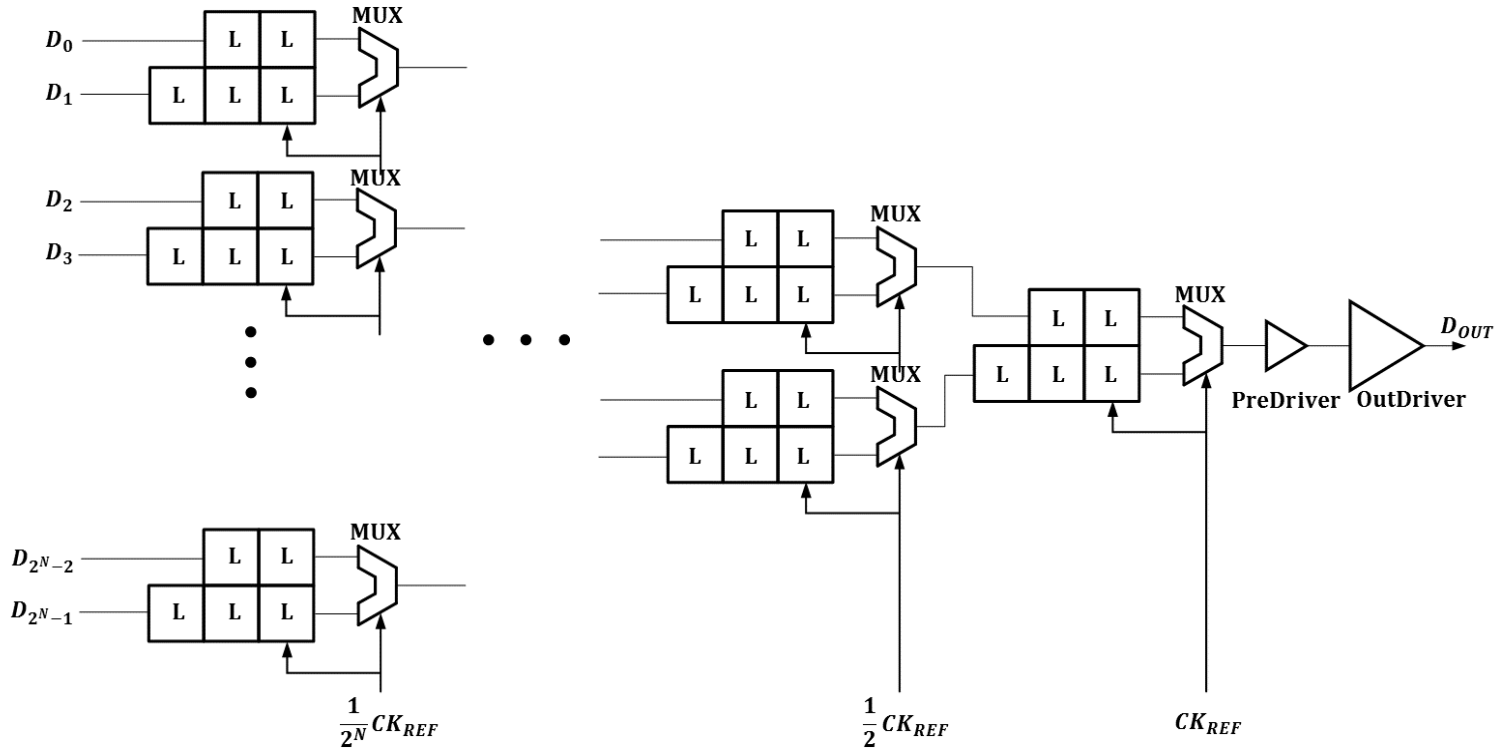


(a) Simple RC model



(b) Proposed delay model

Inter-stage voltage swing optimization



- Various design techniques for improving power efficiency can be easily explored at the top-level model.
  - Example: can we improve power efficiency of I/O by using variable inter-stage voltage swing?

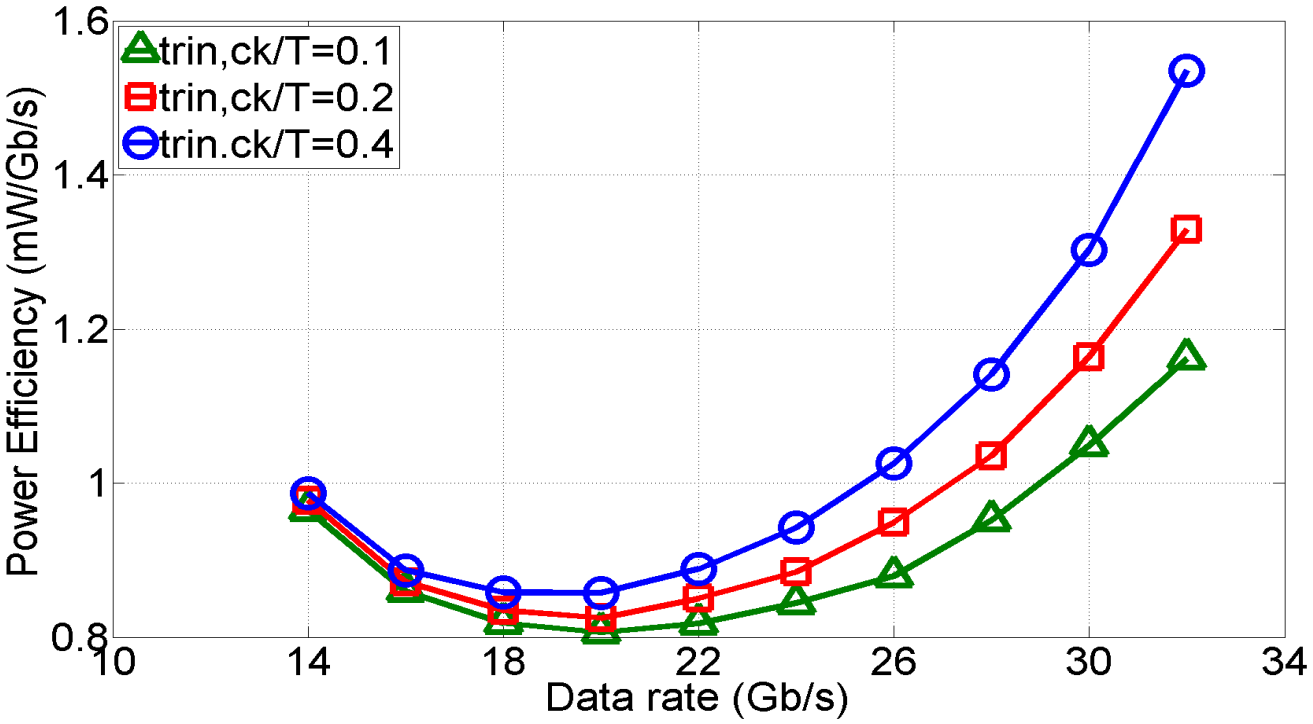
Inter-stage voltage swing optimization

Comparison between varying inter-stage swing and constant swing in sub-blocks at 28 Gb/s

	Variable Inter-stage swing	Constant swing
Power consumption (mW)	26.643	33.370
Power efficiency (mW/Gb/s)	0.952	1.192
Vppd (mV)	400	400
Output jitter (ps_{pp})	0.86	1.09

- **Power efficiency of the transmitter can be enhanced by using variable inter-stage swing.**
  - Signal swing and f_T are simultaneously optimized depending on the different delay constraint s along the serializer chain, leading to 20% improvement in power efficiency.

Optimal Power and Data Rate

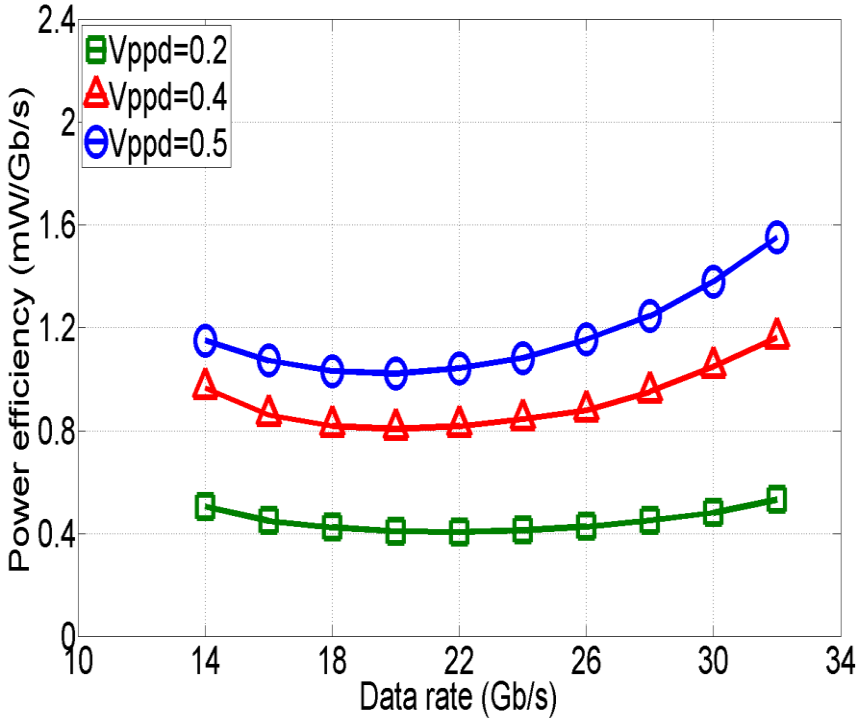


Optimal transmitter power efficiency versus data rate when $t_{r,ck}/T$ is (a) 0.1 (b) 0.2 (c) 0.4 when Vppd is 400mV

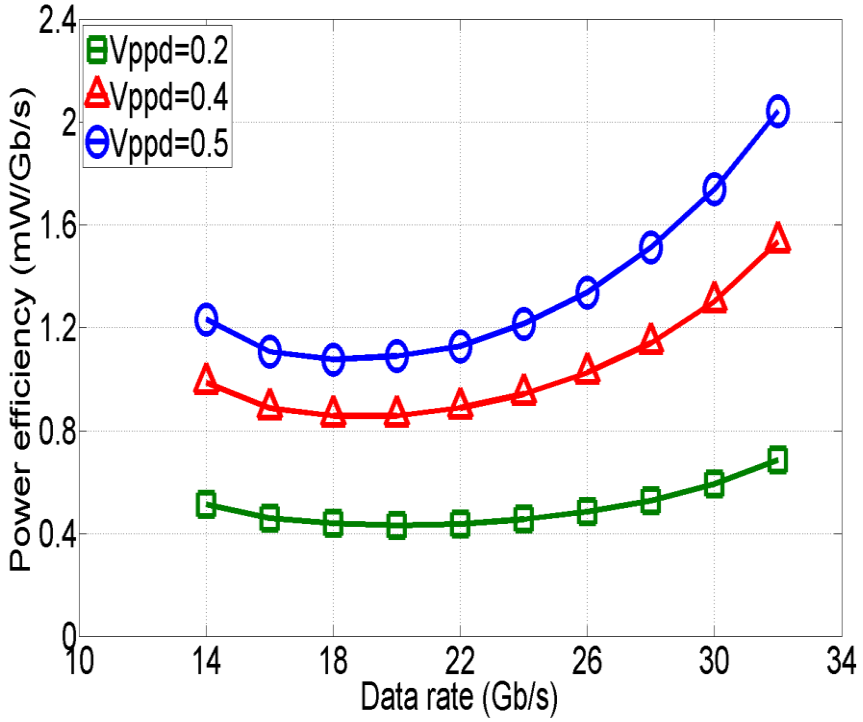
- **Power penalty can be estimated by slowing down input clock transition time.**
- **Optimal data rate can be found to maximize power efficiency.**

Optimal Power and Data Rate

Vppd ↑, Clock transition time ↓ ⇒ Power Penalty ↑



(a)



(b)

Optimal transmitter power efficiency versus data rate when $t_{rin,ck}/T$ is (a) 0.1 (b) 0.4

Conclusion

- We presented accurate CML circuit models compatible with geometric programming
- The modeling involves iterative GP optimizations to refine the accuracy, leading to ~5% mean delay modeling error
- The models can be used in a GP-compatible system-level model as demonstrated using a high-speed link transmitter
- The system-level model can be efficiently synthesized for various design specifications & processes
- Can explore intricate system-level design tradeoffs, providing valuable design guidelines

Reference

[1] M. Hershenson, et al, “Optimal design of a CMOS opamp via geometric programming,” IEEE Trans. Comput.-Aided Design, vol. 20, no. 1, pp. 1-21, Jan. 2001

[2] D. M. Colleran, et al, “Optimization of phase-locked loop circuits via geometric programming,” Proc. IEEE Custom Integrated Circuits Conference, 2003. pp. 377-380, 2003

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[5] U. Seckin, et al, “ A Comprehensive Delay Model for CMOS CML Circuits,” IEEE Trans. Circuit. Syst. Ⅰ. Reg. Papers., vol. 55, no. 9, pp. 2608-2618 Oct, 2008

[6] S. Y. Kim, et al, “Closed-form RC and RLC delay models considering input rise time,” IEEE Trans. Circuit. Syst. Ⅰ.Reg. Papers., vol. 54, no.9, pp 2001-2010, Sep. 2007

[7] R. Mita, et al, “Propagation delay of a RC chain with a ramp input,” IEEE Trans. Circuits. Syst. Ⅱ, Exp. Briefs., vol. 54, no. 1, pp. 66-70, Jan. 2007.

Thank You