Evaluation of a Benchmark Suite for Formal Verification of Analog Circuits

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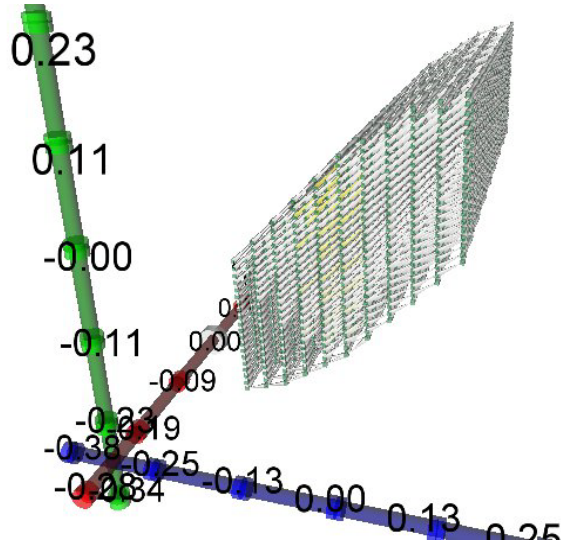
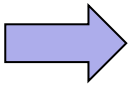


Introduction

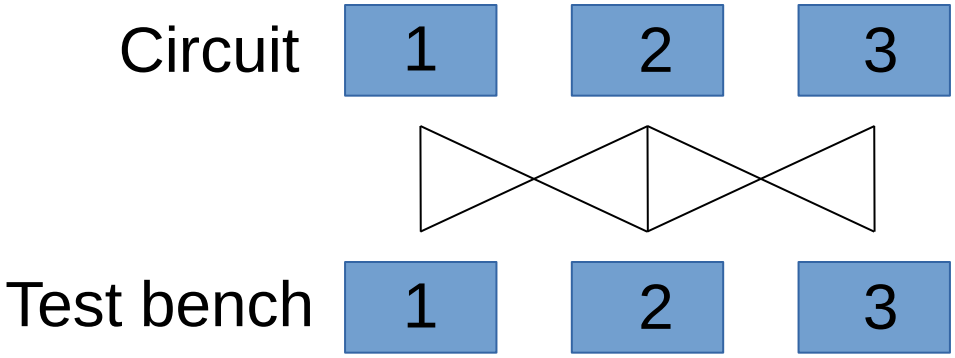
- **MCNC benchmark**
  - **Analog simulation**
  - **Numerical challenges**
  - **Big circuits**
- **ISCAS'89 benchmark**
  - **Digital circuits**
  - **Simulation, verification**



No benchmark available for cross level behavioural model validation and model checking

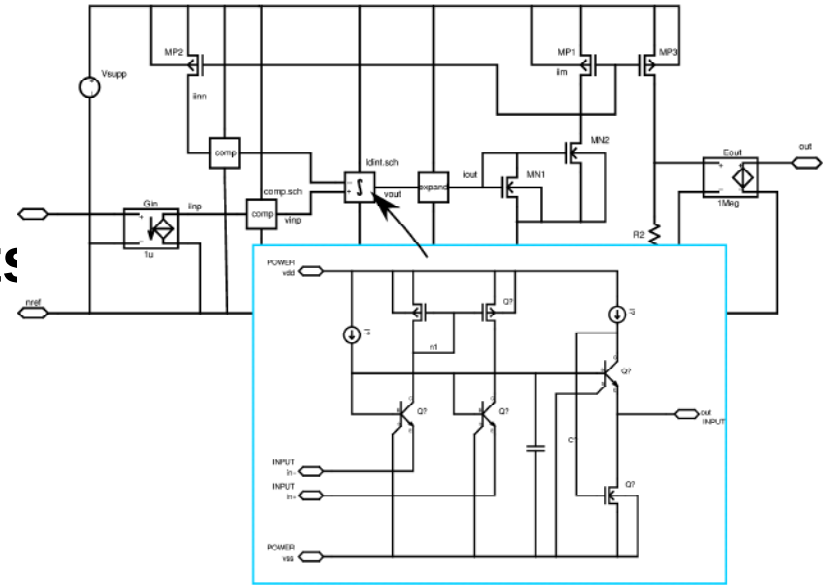
Benchmark Suite for Formal Verification of Analog Circuits

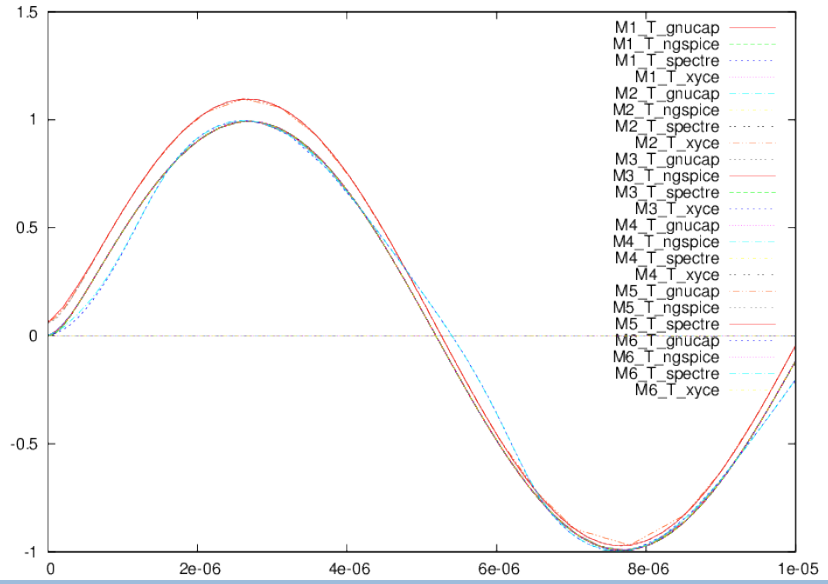
- **Criteria for Selection**
  - Test instances for established methods
  - Challenges for formal methods
  - Proving grounds for new algorithms
  - Portability
  - Pluggability
- **Goals**
  - Share examples
  - Demonstrate results
  - Discussion
    - Terminology
    - Usefulness
    - ...



Supported platforms

- **Test benches and components**
  - Spice netlists
  - Spice macro models
  - Verilog-A modules
  - PTM 180nm parameters

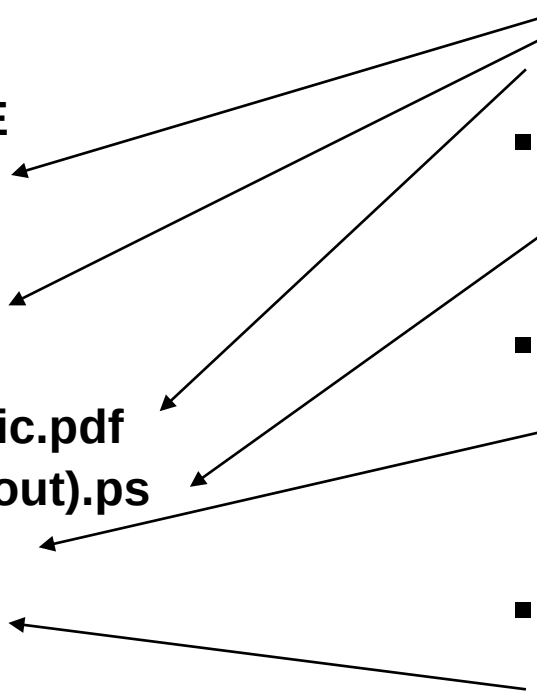




- **Verified to work with**
  - Gnucap
  - Spectre (R)
  - Ngspice*
  - Xyce*

Benchmark Suite: Structure

+ benchmark/
- lowpass/
+ ota/
README
M1.sp
M2.sp
T1.sp
T2.sp
schematic.pdf
T_tr_v(nout).ps
ec.msl
mc.msl
[..]
- ring_osc/
- sigma_delta/

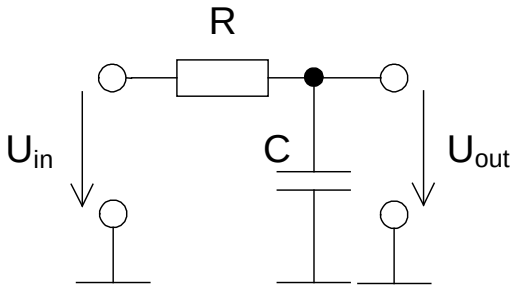


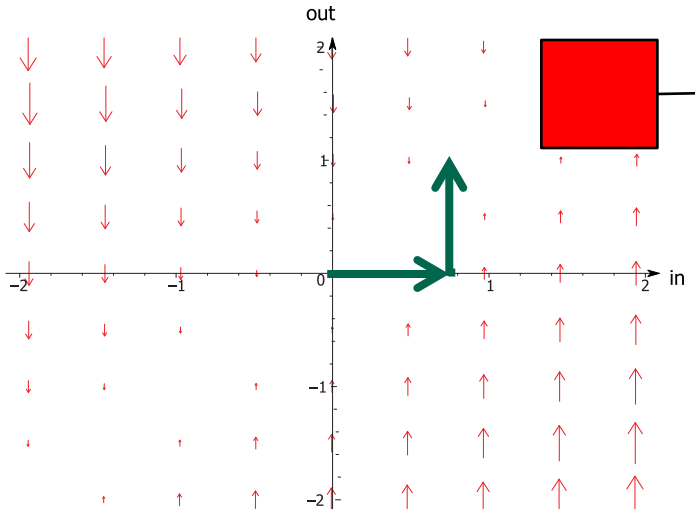
- Modules and Testbenches
  - Different variants
  - Schematics included
- Simulation results
  - Circuit sanity check
  - ensure simulator capabilities
- Equivalence Checking
  - Information on
    Ports, States, Ranges
  - Live example
- Model Checking
  - Information on
    Ports, States, Sets,
    CTL-Formula and ASL-Formula

Benchmark Suite: Circuit examples

Class	Architechture	Implementation	Nonlinear	Inputs	Dim	red. Dim
4-Pole ring oscillator	CMOS interter cells	BSIM, Spice	X	-	4	4
Low pass	RC	Spice, Verilog-a		1	1	1
	RL, gyrator+C coil substitute	Spice-macro		1	1	1
	Log domain filter	Spice, BSIM, BJT	X	1	8	1
	Nonlinear RC	Spice-macro	X	1	1	1
	OTA, active	Spice	X	1	11	1
High pass	similar	similar	X	1	1	1
Band pass	Active (OP)	Spice/BSIM	X	1	8	2
	Active (OP)	Spice/Verilog-A(OP)	X	1	3	2
Operational Amplifier	Miller	Spice/BSIM	X	2	6	1
	Behavioural model	Verilog-A	X	2	1	1
Operational transconductance Amp.	Two stage	Spice/BSIM	X	2	7	1
	Behavioural model	Verilog-A	X	2	1	1
Sigma Delta ADC	Second order	Spice-mactro	X	1	4	1
Inverter, NAND	CMOS	Spice/BSIM	X	1	1	1
Tunnel diode oscillator	TD test bench	Spice-macro	X	-	2	2

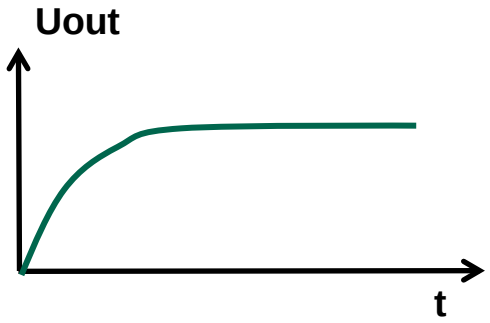
Validation Methods: Simulation, Affine-, Assertion based Verification





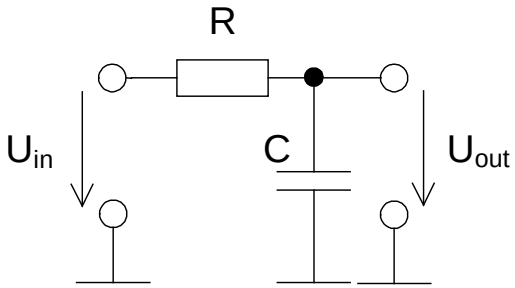
State Space

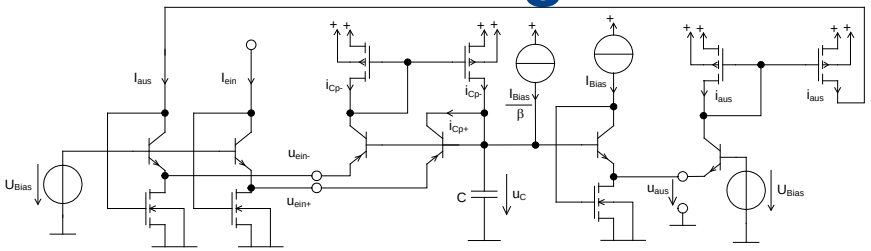
Assertion-based Verification



Simulation

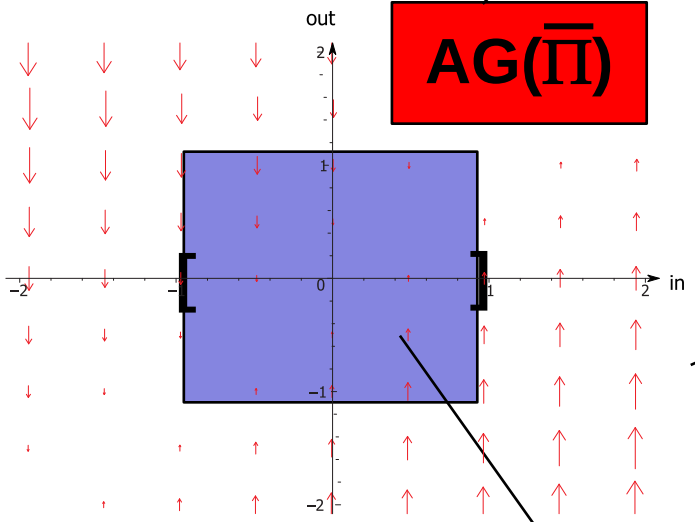
Validation Methods II: Rechability, Model-,Equivalence-Checking

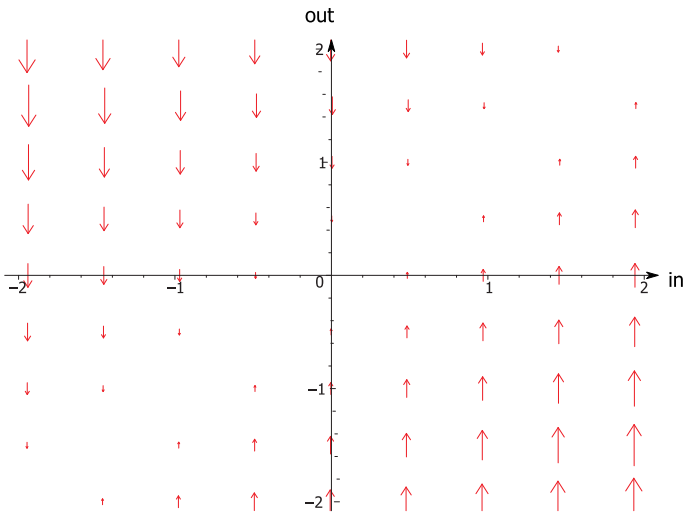




Model-Checking

AG($\overline{\Pi}$)

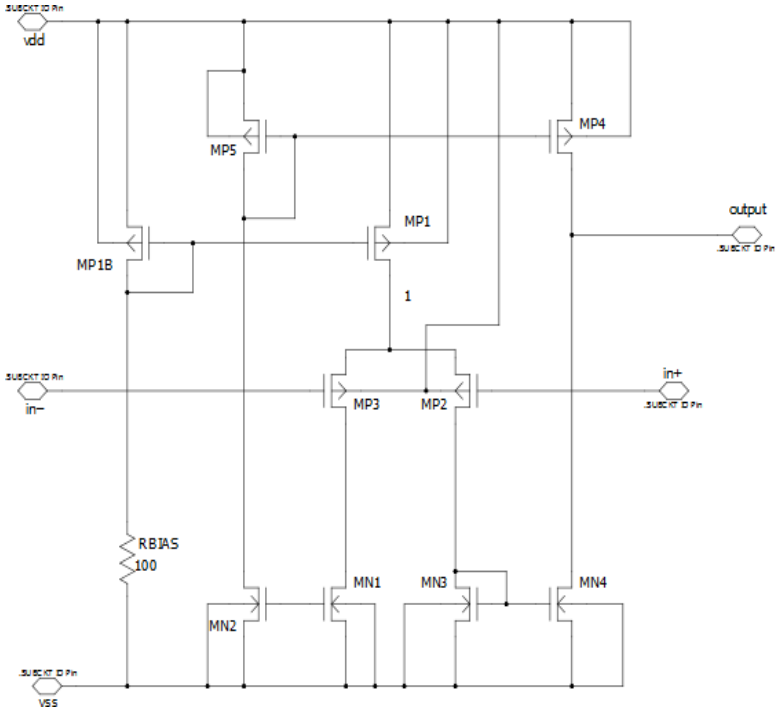




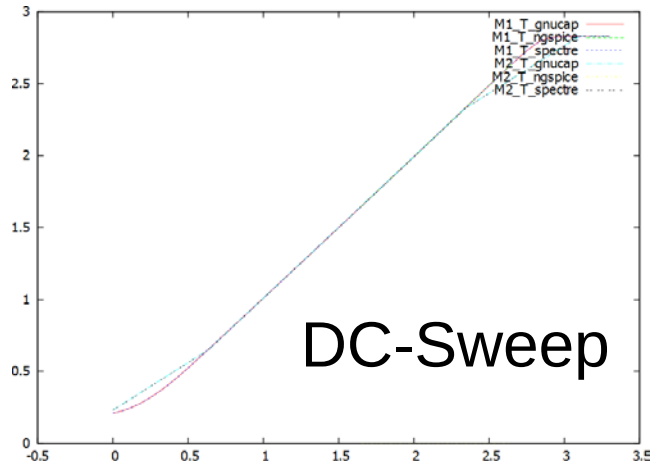
State Space

Reachability

Operational Transconductance Amplifier (OTA)

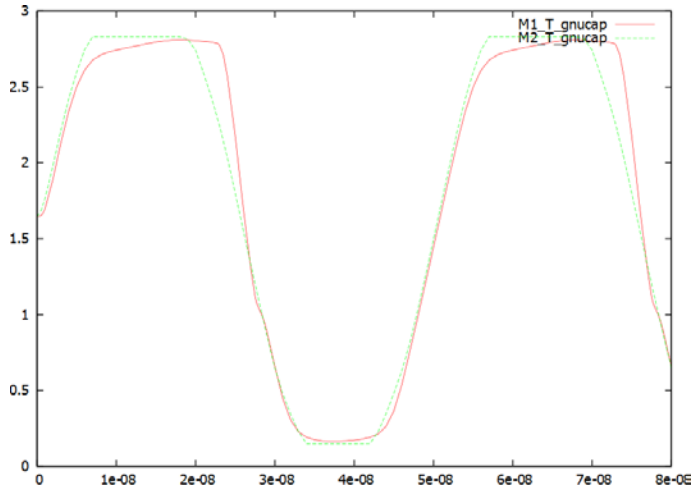



```
analog begin
    I(vddn,out) <+ gm * (V(inp,inn)-voff); // wanted current
    I(vddn,out) <+ cmrr * ((V(inp) +V(inn))/2.0 -
    V(vddp,vddn)/2.0);    // CMRR
    I(out,vddn) <+ V(out,vddn) / rout; // Internal resistor
    I(out,vddp) <+ V(out,vddp) / rout;
    I(out, vddn) <+ C1 *ddt(V(out, vddn) );
    // finite output swing
    if( V(out,vddp) + cloffp  > 0 )
            I(out, vddp) <+ ( V(out,vddp) + cloffp )  / rclamp2;
    if( V(out,vddp) + doff +cloffp > 0  )
            I(out, vddp) <+ (V(out,vddp)+ doff + cloffp) /
    rclamp;
```

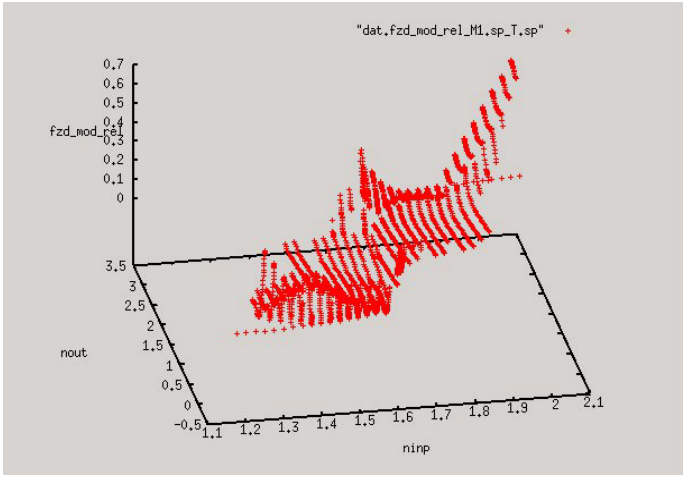


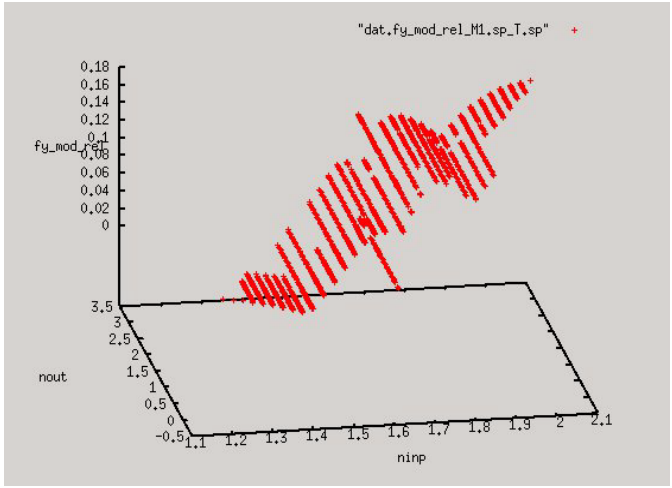
OTA : Equivalence Checking

TR-Simulation



Equivalence-Checking





- **Static error: < 20%**
- **Dyn. error:**
  - **< 70% (up to 25Mhz)**
  - **< 10% (up to 1MHz)**

OTA: Model Checking

Specified and checked properties:

- **Gm , Linearity** **0.003 1/Ω < Gm < 0.005 1/Ω**
- **over shoot** **<10%**
- **under shoot** **<10%**
- **rise time** **< 5e-8 s**

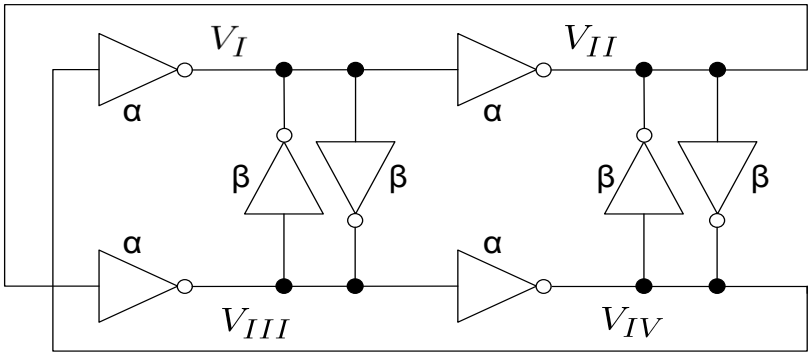
Low Pass Filters: Model Checking

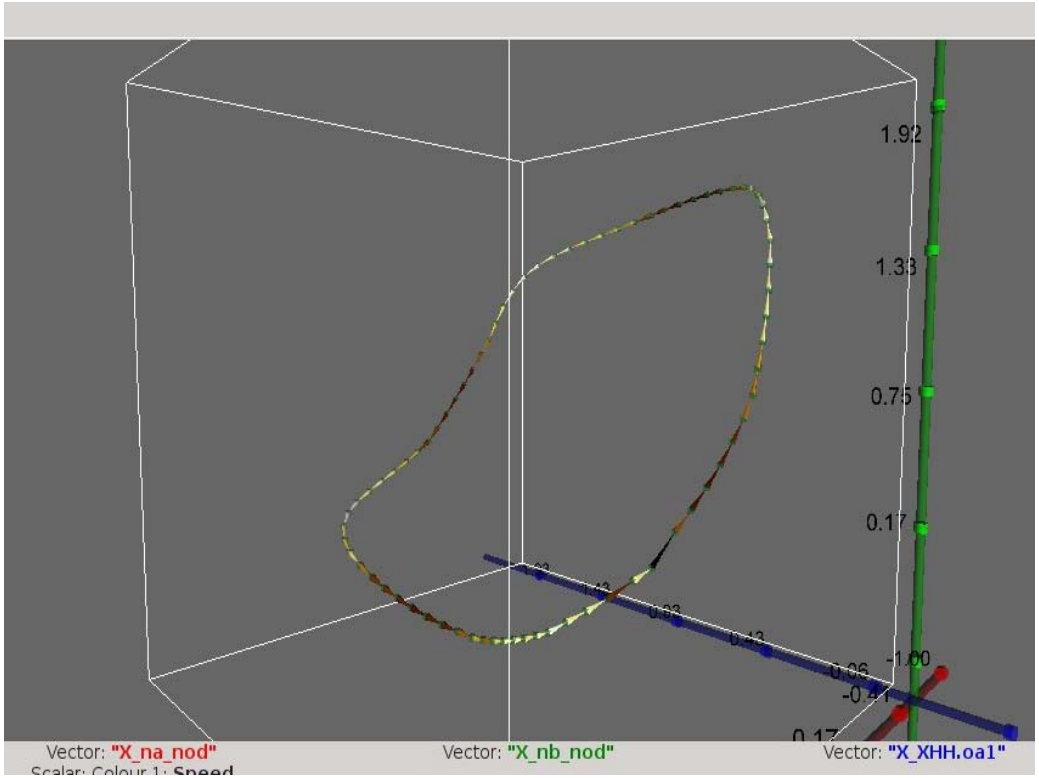
- **MC Properties**
  - **Reachable Area**
  - **Overshoot**
  - **Gain**
  - **Slewrate**
  - **Step response**

  … counter examples
- **Variants**
  - **RC, LR**
  - **Nonlinear C RC**
  - **LR with gyrator and Cap**
  - **Logdomain**
  - **OTA (active)**

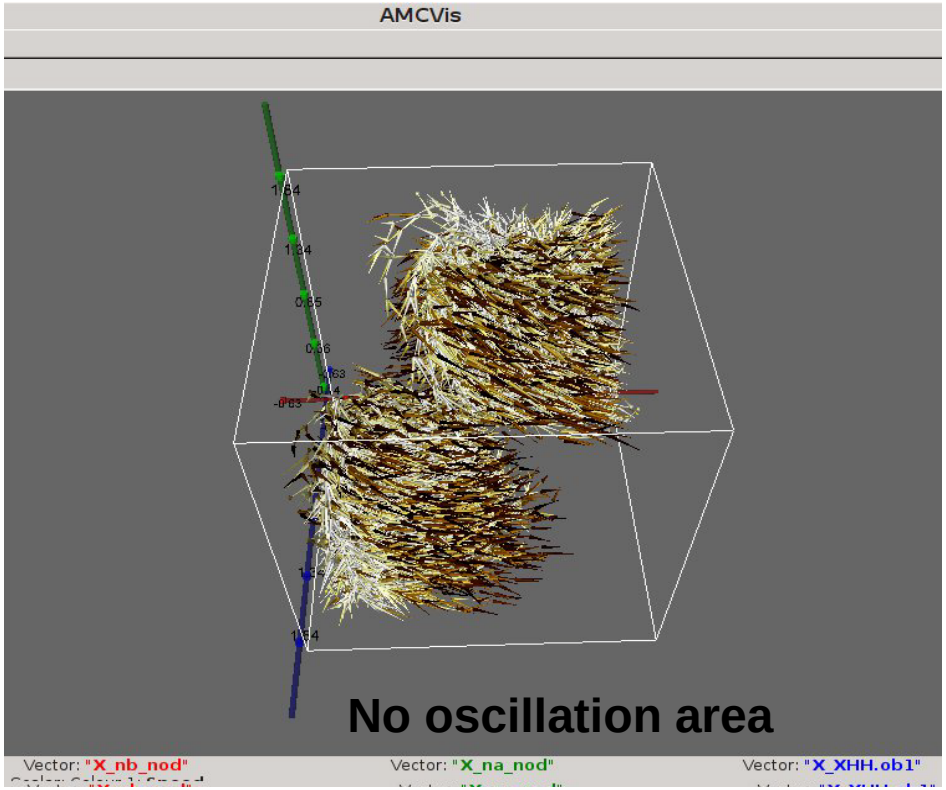
```
# Reachable states
fix = steadystates;
reachable = EF^-1 fix;

# Reachable states from  -0.1 < Uin < 0.1
uslice = nin[<0.11] and nin[>-0.11];

ulow = nin[<-0.09] and nin[>-0.11];
uhigh = nin[<0.11] and nin[>0.09];

reachin = on uslice reach from fix;

# overshoot
overshoot = reachin and nout[> 0.12];
undershoot = reachin and nout[< -0.12];

# dc-gain of odB:
calculation gain_calc("(calc_par3 – calc_par4)/  \
                       (calc_par1 - calc_par2)");

numvar %gainmin,%gainmax;
on fix assign(%gainmin,min)
   gain_calc(nin,0,nout,0)[-inf,inf];
on fix assign(%gainmax,max)
   gain_calc(nin,0,nout,0)[-inf,inf];

for %gainmin assert [ 0.8, 1.2 ];
for %gainmax assert [ 0.8, 1.2 ];

[..]
```

4-Pole Oscillator at α/β = 2.4





Oscillation trajectory



Evaluation

Class	Architechture	Implementation	Nonlinear	Sim	EC	MC
4-Pole ring oscillator	CMOS interter cells	BSIM, Spice	X	X		X
Low pass	RC	Spice, Verilog-a		X	X	X
	RL, gyrator+C coil substitute	Spice-macro		X	X	X
	Log domain filter	Spice, BSIM, BJT	X	X	X	X
	Nonlinear RC	Spice-macro	X	X	X	X
	OTA, active	Spice	X	X	X	X
High pass	similar	similar	X	X	X	
Band pass	Active (OP)	Spice/BSIM	X	X	X	
	Active (OP)	Spice/Verilog-A(OP)	X	X	X	
Operational Amplifier	Miller	Spice/BSIM	X	X	X	X
	Behavioural model	Verilog-A	X	X	X	X
Operational transconductance Amp.	Two stage	Spice/BSIM	X	X	X	X
	Behavioural model	Verilog-A	X	X	X	X
Sigma Delta ADC	Second order	Spice-mactro	X	X		
Inverter, NAND	CMOS	Spice/BSIM	X	X		
Tunnel diode oscillator	TD test bench	Spice-macro	X	X		X

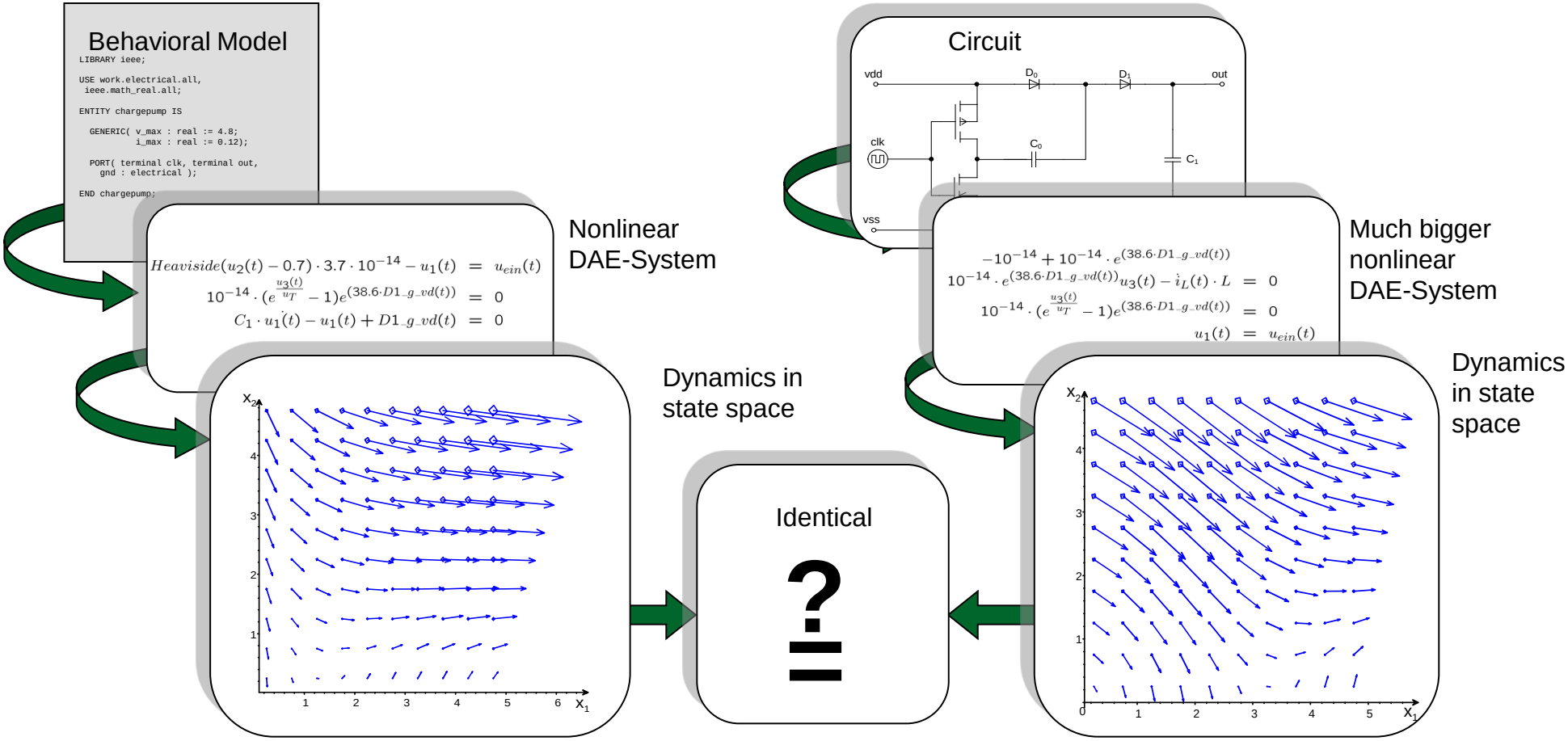
Conclusion

- **Benchmark suite available***
- **Key issues addressed**
  - **Model checking**
  - **Equivalence Checking**
  - **Transistor and behavioural level**
- **Unaddressed Problems**
  - **Process Variablility**
  - **Mixed Signal**
  - **System Level**
  - **Extracted Circuits**
- **Contributions welcome!**
  - **salfelder@em.cs.uni-frankfurt.de**

***http://www.em.cs.uni-frankfurt.de/FAC14/benchmark**

Thank You

Equivalence Checking Concept



- Use gnucap simulator as back end.

- 50 equations/transistor
- Implicit, strongly nonlinear equations
- Use of numerical evaluation

Model Checking Flow