System-Level Operating Condition Checks: Automated Augmentation of VerilogAMS Models

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***Abstract*—Analog/Mixed-Signal (AMS) design and verification strongly relies on more or less abstract models to make extensive simulations feasible. Maintaining consistent behavior between system model and implementation is crucial for a correct verification. This also involves the operating conditions: A faulty model might introduce false-positive verification results despite of e.g. an incorrect supply voltage or missing bias currents. We present an automated workflow for extracting these checks from a transistor-level implementation and transfer it into a given Verilog-AMS model. The correctness of our approach is proved by evaluating the model coverage between the implementation and the model.**

Operating Conditions on System-Level?!

A very important step in top-level verification is to ensure that each component in the system in its safe operating area. For instance, a transistor has to be operated in a way that does not cause damage to the specific device. We define the acceptance region of a model as the region in the parameter space where the component complies to its specification [1]. This parameter space comprises every relevant quantity influencing the block's behavior. Hence, the operating condition check on this level has to observe the current environmental parameters and classify whether the current conditions are within the acceptance region. We extract this acceptance region of the transistor-level circuit using the methods shown in [1]. This region is represented using a Support Vector Machine (SVM). This allows the region to be expressed as a decision function that can be a also described in Verilog-AMS. For that purpose, we use an automated scheme [2] to automatically create this additional module and insert it into a given Verilog-AMS model. In this way, the operating condition check can be executed from within the simulation enabling the model to react to the current environmental situation.

For checking if the model is currently operating in an acceptance region, we create a Model Safe-Guard Unit (MSU) as shown in Fig 1. This unit comprises three elements. Sensors are used to supply the environmental conditions of the block to the classifier representingthe knowledge about the acceptance region of the transistor-level circuit. It is automatically trained with simulation data of the transistor level circuit. The output of the classifier is passed to one or more actuator blocks that are used to react to the current conditions as for instance raising error messages or modifying the models output signals. To generate Verilog-AMS code, we use a text-templating approach. The generated elements are assembled using a code-rewriting framework as shown in [1]. This framework is also used to integrate the MSU with an existing Verilog-AMS model of the block. Like this, the fully-automated flow is realized. For demonstrating our method, we use a component of a passive HF-RFID communication path simulated in Cadence AMS Designer. To verify if the system is operating properly within the acceptance region, an extensive simulation has to be executed. With our method, we are able to execute this simulation using Verilog-AMS models while still including the knowledge about the acceptance regions and therefore integrated system-level operating condition checks.

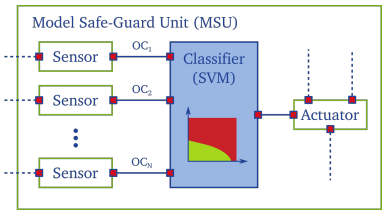

Fig. 1. Structure of the generated checker module

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