Detecting Design Flaws using Analog State Space Coverage

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Abstract

Today, analog circuit design and verification needs sophisticated designers and verification engineers to prevent faulty behaviour and expensive redesigns. While analog designs getting more and more complex, a metric describing the coverage of an analog circuit is needed. Coverage metrics are convenient instruments in the digital design, but lacks in a formal description in the analog design field. An analog coverage metric would help to guide a designer into areas not considered by tests before. One way to archive a high coverage (and therefore a *safe* implementation) is to run a lot of simulations which does not guarantee to inspect every region of the device under test, but uncovered scenarios could lead to massive problems in the later production of the chip. Our goal is to define a measure to score a given simulation and later on increase the coverage of the overall test scenario. We will show that this is possible in a fast way, without missing possible design flaws at all.

First of all, we will start with a discrete state space of a given analog circuit design, which is computed from a transistor netlist with BSIM accuracy, consisting of a set of states and transitions between those states [1]. A transient simulation response is then mapped to the set of states, describing a coverage of the device under test. Since the discrete state space can be stored as a weighted graph structure, an A^*- search [2] is used to find paths through the graph by avoiding already visited states. These generated paths are used to create new input stimuli for the simulator. The full coverage maximization algorithm is shown in Fig. 1.

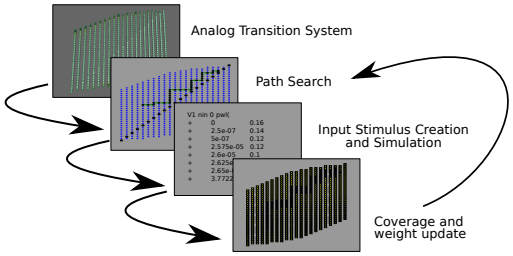

Fig. 1: Coverage maximization algorithm based on a discrete state space.

Trying to create all stimuli for more and more complex analog circuits is obviously futile and visiting every state of a discrete state space does not make sense at all. Reducing the number of states without increasing the probability to miss a bug is achieved by visiting only important states of the system. To detect these regions, we are segmenting the discrete state space in regions with uniform (linear) behavior which only needs one simulation trajectory through this region to ensure the correctness of the implementation. By contrast, as analog systems also exhibit non-linear parts with high dynamic (such as limited output voltage swings), these regions need to be thoroughly visited under all circumstance as the probability for faulty behavior in these nonlinear regions is much higher than in uniform linear regions. For distinguishing uniform linear from nonlinear non-uniform regions, the eigenvalues captured in the states of the analog transition system are used (see Fig. 2 and [3]). Based on this informations, the graph of the system is updated, leading in a much more precise path searching algorithm. Experiments shows that similar accuracy can be reached by a significant speed-up compared to the basic algorithm described before and that the methodology can uncover overseen flaws.

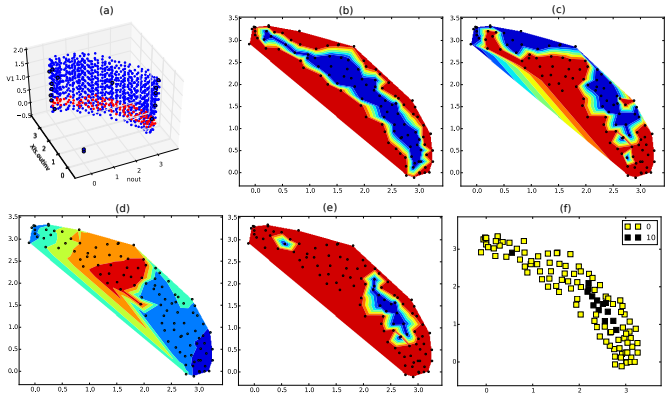

Fig. 2: Results of the state space analysis of a level-shifter circuit: (a) shows the set of reachable states. The border regions (b) and the dynamics (c) based on the eigenvalues of the system (d) are combined to a weight visualized in (e). Yellow points in (f) show interesting points to be covered.

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References

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