Formal Verification of Analog Circuits (FAC) '08

A satellite workshop at CAV 2008

July 14th, 2008, Princeton, US

Organizers: Oded Maler and Lars Hedrich

Monday, July 14, 9:00-12:20	
Invited talk 9:00-10:00	**Temporal Testers: The Building Blocks for Verification Automata** Amir Pnuel (New York University, USA and Weizmann Institute, Israel)
1 10:00-10:40	**Analog Property Checkers: A DDR2 Case Study** K.D. Jones and V. Konrad (Rambus Inc. USA) D. Nickovic (Verimag, University of Grenoble, France)
Break, 20min	
2 11:00-11:40	**A Bond Graph Approach for the Constraint based Verification of Analog Circuits** W. Denman, M.H. Zaki and S. Tahar (Concordia University, Canada)
3 11:40-12:20	**Abstract Modeling and Simulation Aided Verification of Analog/Mixed-Signal Circuits** S. Little and C. Myers (University of Utah, USA)

Monday, July 14, 14:00-17:00	
4 14:00-14:40	**fSpice: A Boolean Satisfiability Based Approach to Formally Verifying Analog Circuits** S.K. Tiwary, A. Gupta, J.R. Phillips, C. Pinello and R. Zlatanovici (Cadence Research Labs, USA)
5 14:40-15:20	**Statistical Model Checking of Mixed-Analog Circuits** E. Clarke, A. Donze and A. Legay (Carnegie Mellon University, USA)
Break, 20min	
6 15:40-16:20	**Structural Methods for Equivalence Checking of Analog Circuits with Strong Nonlinearities** L. Hedrich and S. Steinhorst (University of Frankfurt/Main, Germany)
Invited talk 16:20-17:00	**A Digital Verifier's Peek into the Analog World** Victor Konrad (Rambus Inc. USA)